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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 10/81)

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USSR REPORT

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 10/81)

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HARDWARE

UDC 621.326.3

CAMAC CONTROLLER FOR THE ELEKTRONIKA-60 COMPUTER WITH INTERNAL PROCESSING OF REQUESTS

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 10-15

[Article by V. Ye. Soloboyev and V. I. Solonenko, Novosibirsk]

[Text] In the controllers ordinarily used for the "Elektronika-60" microcomputer the time of response to a request is about 20-25 microseconds (and due to regeneration in the memory that time can reach 180-200 microseconds). In addition, module-to-module transfer of information requires 30-35 microseconds of time. All this greatly limits the possibilities of servicing rapid processes. The task was set of developing a CAMAC crate controller for the "Elektronika-60" microcomputer, which together with the realization of ordinary modes (program and of interruptions) would assure a request response time of less than 1 microsecond and a module-to-module exchange rate of up to 2.5-3 microseconds in a single crate for a certain class of requests.

In developing that controller the following idea was used: that of introducing into the controller its own storage, into which programs for the handling of main line requests are loaded. At the requests of modules the controller must issue necessary control signals with minimum delay from that storage to the crate main line and assure data transmission within the crate. Similar ideas of control function decentralization were expressed earlier (cf, for example, [1.2]), but efficient devices of that type are still not widespread, evidently because of difficulties in their technical realization.

Taken as the basic variant for a controller with internal request handling was the controller developed in the Institute of Automation and Electrometry, Siberian Department, USSR Academy of Sciences [3]. That controller contains all units of the basic one, but the internal request handling mode and its border with other modes were obtained by introducing 35 microcircuits of medium integration in which the storage and necessary control units were realized.

Figure 1 presents a structural diagram of the controller. In it, in comparison with the basic variant, only two units have been added--an address storage register and a main housekeeping program store RNAF, and a control device was also simulated. The formats of the controller registers are presented in Figure 2.

Work in ordinary program and interruption modes is not examined in detail here, as it was described in [1]. In the internal request handling mode all requests

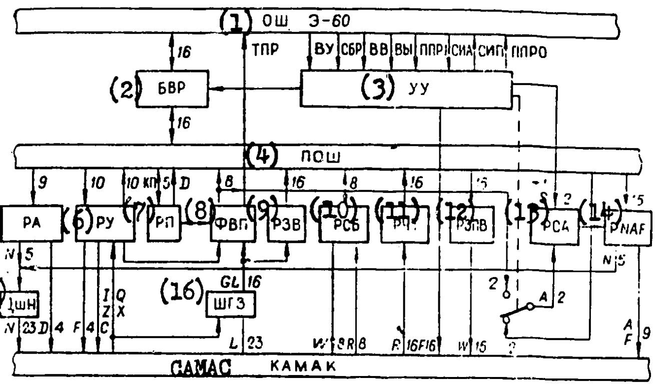

Figure 1. Structural diagram of collector.

1 -- E-60 computer common bus
2 -- buffer valve register
3 -- control device
4 -- pseudo-common bus
5 -- address register
6 -- control register
7 -- priority register
8 -- discontinuity vector former
9 -- valve request register
10 -- senior byte register
11 -- readout register
12 -- valve recording register
13 -- address counter-register
14 -- NAF register
15 -- number (station) decoder
16 -- group request decoder

for priority level recorded in the controller priority register are divided into two groups, the external and internal (in the ordinary discontinuity mode these are the permitted and unpermitted); the following system of priorities, taken in the "Elektronika-60" computer, is extended to all requests; modules more remote from the controller have a lower priority. When the priority level is lowered, internal requests will be translated into external, starting with the greater priorities. Modules which must be serviced in the internal request handling mode are allocated places with lower priority in the crates.

External requests, as in an ordinary controller, are serviced by computer. Internal questions are handled without direct participation of the computer. The internal request handling mode is included (after the housekeeping program has been recorded in the NAF register) when "1" is recorded in row M1 of the controller control register, and is removed when any reference is made to that crate (during the request waiting time) or when an external request appears.

The housekeeping program is recorded in the NAF register in the following manner: a) for the subaddress A(5) the initial address is recorded in the RSA; b) for subaddress A(7), series NAF of the housekeeping program (after each registration the address is automatically increased by 1). To monitor the content of the NAF register the possibility of its readout is provided for. Figure 3 presents a block diagram of the internal request handling unit.

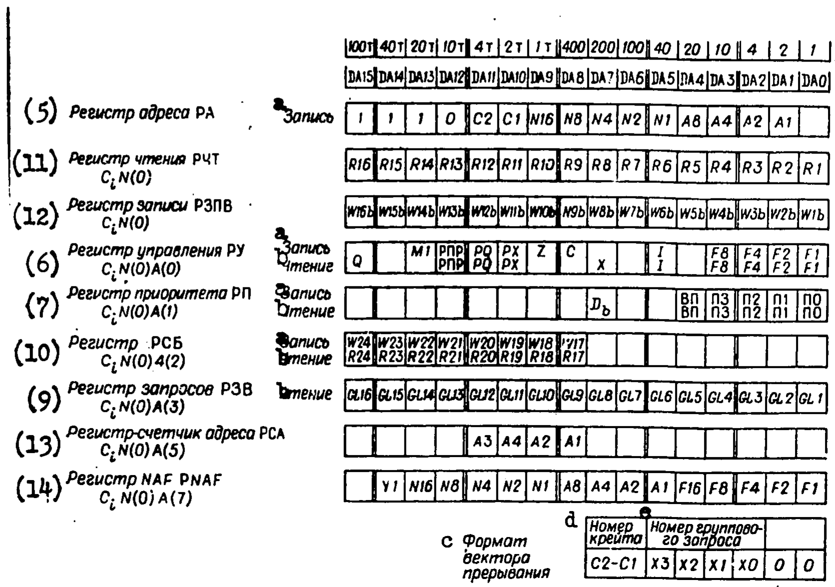

Figure 2. Formats of controller registers.

a - Recording
b - Readout
c - Format of discontinuity vector
d - Crate number
e - Group request number
Numerical keys same as for Figure 1.

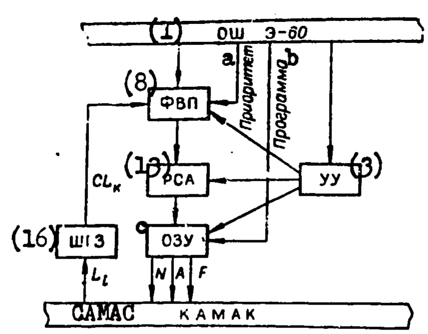

Figure 3. Block diagram of controller with internal request processing.

a - Priority
b - Program
c - Main storage

Numerical keys same as for Figure 1.

The controller functions as follows after transition into the internal request handling mode. Upon appearance of a request which must be serviced in the internal request handling mode, the code from the output of the interruption vector former is recorded in the address counter-register as the starting address of the subprogram for the servicing of that request. For that initial address the first control word of the housekeeping program is summoned from the storage. The control unit produces the first CAMAC cycle, according to which the module selected by the control word performs the required operation (the control word contains the module number N, its subaddress A and the operation F). Besides NAF, the control word contains the instruction digit Y1. If in that digit "1" is written, after the first CAMAC cycle follows a second cycle during which on the main line a new NAF will be produced, read from the next storage cell. The described process will be repeated until the moment when "0" appears in digit Y1; after performance of the last NAF the controller goes over into the mode of awaiting a new request.

During the servicing of internal requests the controller is disconnected from the computer common bus, and this minimizes the mutual interference of the controller and computer.

In the internal request handling mode several requests can be handled by multiple repetition of the NAF chain (for example, in the drawing of a graph on a CRT). If during the handling of such a request a request with a higher priority appears, it starts to be handled after completion of the NAF chain. If the request has arrived from the zone of external request, after completion of the NAF chain the external requenst handling mode will be removed, the controller produces a KTPR signal and changes to the ordinary handling mode by means of the computer.

At least one active module must be provided for automatic emergence (without computer participation) from the internal request handling mode in the crate (in that case the request of that module must be related to the area of external requests). Emergence from the internal request handling mode can also be accomplished upon request, formed in the controller upon appearance of the signal Q. Let us note that provision must also be made in the crate for facilities for the assignment and storage of constants, for example, the tumbler register modules.

The main storage used on K155RU2 microcircuits (4 each) has a capacity of 16 15-digit words and permits servicing 4 internal GL0-GL3 requests with an NAF quantity of up to 4 in the housekeeping program of each request. Those 16 words form in the storage four regions with their own initial addresses (Figure 4). If a larger number of NAF is required for the servicing of any address at all, a region of the storage of adjacent requests can be used if it is not used in the given experiments. In our opinion, four internal requests are completely adequate for the servicing of a large number of experiments.

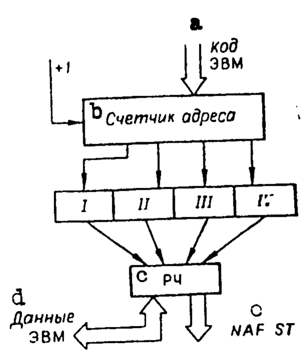

Figure 4. Distribution of housekeeping programs in the storage.
a -- computer code
b -- address counter
c -- number counter
d -- computer data
e -- NAF signal of end of housekeeping program.

In cases in which several modules generating requests are used in the crate but their housekeeping programs are run in turn (for example, the accumulation of information and visualization), it is advisable to store the internal requests housekeeping subroutines in the computer main storage and fill them with the controller storage at the necessary mlments of time. If the modules generating requests cannot for any reasons be set in position with the ordered requests GL0-GL3, then in that situation a replaceable coder of ordered requests should be used. In principle it is possible to increase the storage volume for the servicing in an internal request handling mode of 16 ordered requests used in the controller, but that does not seem necessary.

In the case where subroutines for internal request servicing are stable and do not vary it is possible to use an ROM instead of a storage unit in the controller, which will simplify the controller and work with it.

Some difficulties arise in the use of the described controller if the module contains several sources of requests. To service these requests in internal request handling mode, they can be spatially divided. In that case it is advisable to bring the additional requests out on the front panel and through auxiliary modules (established in a desirable position of the crate) feed them to the crate main line. This method permits the controller to run branching programs, determining the direction of branching from the sources of requests within the module.

On the basis of the examined structural diagram a model of a controller with internal request handling has been developed, made and debugged, one completely satisfying the requirements of EUR 4100 and specifications of the "Elektronika-60" computer common bus.

To verify the working capacity and illustrate the possibilities of a controller with internal request handling, a system for data collection and visualization was assembled which included the following modules: a 10-bit analog-digital converter; a main storage of 4K 16-digit words; a 10-digit digital-analog converter; a starting pulse generator; a 1 TR1 tumbler register which assures selective setting of the counter mask trigger; a 2 TR2 tumbler register which sets the array length; a 3 TR3 tumbler register which sets the initial address of the main storage; a counter register (of the array length) and also an oscillograph and sine-wave signal generator.

The system assures analog-digital conversion of data, their remembrance in the storage and their withdrawal by means of a digital-analog converter to an oscillograph for observation. The work of the system proceeds in two stages: I -- accumulation of data from the analog-digital converter; II -- visualization.

The equipment is started by the pushbutton of the starting generator, which generates a pulse which starts the analog-digital converter through the front panel.

Upon the appearance of a request from the analog-digital converter a series of NAF instructions is issued from the NAF register which assures data readout from the analog-digital converter, its starting and erasing of the request, the registration of data from the controller in the main storage and deduction of a unit from the contents of the counter-register. Upon completion of the analog-digital conversion a new request develops from the analog-digital converter.

Those chains will proceed at a ratė determined by the conversion time of the analog-digital converter until in the counter-register the content becomes unequal to 0, which summons a request from the counter-register. The counter-register is set in such a position that its request is external. On the basis of that request the internal request handling mode will be removed and the computer will perform preparatory operations necessary for data visualization.

On the basis of a request from the counter-register, which was not yet removed during emergence from the internal request handling mode, the controller issues a series of instructions which assure preparation of issuance of a single realization of data from the oscillograph. Then on the basis of a request from the generator, which is switched on by a tumbler on the front panel, the controller issues a series of instructions necessary for issuance of each readout to the oscillograph.

As soon as a single realization is brought out to the screen from the storage, the process will be repeated cyclically on a new request from the counter.

Thus, after connection of the generator a picture of the registered process is visible on the oscillograph screen. By means of tumbler registers TR1 and TR3 the initial address and length of the array can be varied, which permits examining any fragment of the image in details.

Tests have shown the complete working capacity of the controller that has been developed. The results obtained in tests confirm the accuracy and correctness of the technical decisions adopted. At the present time the developed controller has been transferred to experimental operation.

The controller has the following characteristics:

1. The rate of module-to-module exchange is 2.5 microseconds per transfer.
2. The delay time of reaction to a request is not over 250 nanoseconds.
3. The number of internal requests from the crate processed without computer intervention is 4.
4. The number of NAF in the housekeeping program of a single address is 4 (it can be increased to 16 when the number of requests is reduced accordingly).
5. The total number of microcircuits is 110 (mainly with small and medium degrees of integration).
6. Consumption of 2A from the crate 6V power source and of 0.3A from the +5V computer source.

The developed controller assures control of rapid processes and unloading of the computer of routine operations. In some cases, application of the developed controller can assure a simpler realization of the system than when multicontroller systems created in accordance with EUR 6500 are used. The principles built into the controller can be used in the development of controllers for other computers controlling CAMAC.

In conclusion the authors express appreciation to A. I. Yefrimov, who participated in the experimental part of the work.

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CSO: 1863

UDC 681.32

ELEKTRONIKA-60 COMPARISON

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 104-107

[Article by A. Kasperovich, Novosibirsk]

[Excerpts] In the planning of CAMAC systems an important place is occupied by the development of devices which assure handling the requests of modules. The andling of requests (identification, separation of the highest-priority request, change of the priority levels, masking, etc) can be accomplished by either software or hardware); the use of hardware assures a considerable acceleration of handling.

The hardware needed for request handling can be arranged either in special modules (request sorters) [1] or directly in the controllers. Thus, for example, in a controller [2] a device is used which solves the problem of separating and identifying a request of higher priority. Requests arrive in that controller at the input of the sorter which, after analyzing them, issues the interruption vector (the address at which the handling subroutine starts) of the highest-priority request.

A second task, control of the request priorities, can in principle be accomplished by commutation of requests arriving at the controller sorter input. Change of the priority level is desirably done by means of a computer which controls the crate through a controller. Commutation of requests by mechanical switches is not effective and not always convenient.

In the controller's request sorter [3], microcircuits of priority interruption 589IK14 are used to separate the highest-priority request.

In that case when erasure of the discussed request and permission of the new interruption will be accomplished in succession by two computer instructions, with a length of execution of an instruction of more than 6 microseconds (which is valid, for example, for a computer of the Elektronika-60 type), erroneous secondary requests will not arise. Therefore it can be concluded that it is advisable to use such a device to change the priorities of requests in controllers controlled by mini-computers.

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NEW DEVICE DEVELOPED FOR ELEKTRONIKA-60

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980 p 13

[Article by Candidates of Technical Sciences S. I. Yemets and I. F. Khanin and engineers P. P. Kulikov, A. A. Ovdiyenko, and I. D. Petrenko: "Unit for Parallel Exchange of Information with the Elektronika-60 Microcomputer"]

[Text] Contemporary complexes of hardware for automated control systems for industrial processes are created on the basis of broad employment of the latest advances of microelectronics, in particular using microprocessor sets and microcomputers. The Elektronika-60 microcomputer stands out among the computing machines of this class produced by domestic industry. Thanks to its small size, low cost, and program compatibility with the SM-3 and SM-4 computers, it can be used in both local systems and comprehensive automated control systems for industrial processes with decentralized data processing.

The connection of external units to microcomputers is envisioned using the Il parallel exchange devices produced together with the computers. Each of them can connect one external unit working on input-output to the microcomputer. Considering that the maximum load of a channel of the Elektronika-60 microcomputer is 17 standard units, where the standard Console-260, FS-1501, and PL-150 units and a full volume of internal memory are used in a set with the machine, only eight external units can be connected by means of Il devices. In some cases this is plainly inadequate.

A device for parallel exchange of information that converts the internal interface of the Elektronika-60 microcomputer into a coupling interface with the external unit was developed to expand the functions of systems built on the basis of this microcomputer.

The coupling interface with an external unit is organized on the radial mainline principle and includes the following 36 signal lines: 16 two-directional data exchange lines D < 0-15 >; eight address lines for selection of external units A < 0-7 >; one line apiece for strobing the address of the UV's [possibly subtracters] which transmit and receive data; eight interrupt request lines from the external memory units < 0-7 >; one clear external units line.

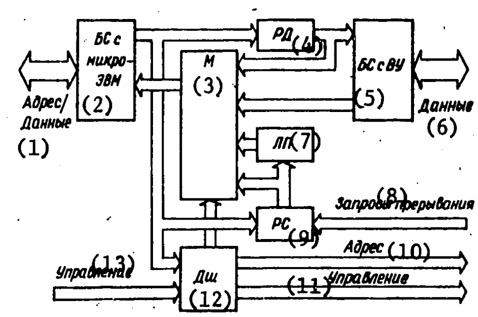
The D < 0-15 >, UV, data receiving, data transmitting, and clear lines are collective; the A < 0-7 > and memory unit < 0-7 > are individual. When the lines are used in this way one parallel data exchange unit permits connecting up to eight external units to the microcomputer, and where the A < 0-7 > lines are used as collective-use lines it is possible to connect up to 256 external unit registers to the device.

The parallel exchange device provides information exchange between the microcomputer and the external units in a program mode and upon interrupt demands from the external units.

Through the use of two-directional data exchange lines with the external units the total number of external interface lines was reduced in comparison with the number of external lines of the I1 device.

Data may be transmitted from the microcomputer to external units in 16-bit words and bytes (higher-order and lower-order); data can be received from the external units only in 16-bit words.

Figure 1 below shows a structural diagram of the device. The coupling buffers with the microcomputer and external units are built with K589AP26 and K589AP16 elements respectively and provide two-directional data exchange.



Key:
(1) Address/Data;
(2) Buffer Coupling with Micro-Computer;
(3) Multiplexor;
(4) Data Register;
(5) Buffer Coupling with External Units;
(6) Data;
(7) Interrupt Logic;
(8) Interrupt Request;
(9) State Register;
(10) Address;
(11) Control;
(12) Decoder;
(13) Control.

Figure 1. Actual Diagram of the Unit

The levels of the signals in the lines of the microcomputer are: logical "1" — + (0-0.8) volts; logical "0" — + (2-3.4) volts.

The signal levels in the lines of the coupling interface with external units are: logical "1" — + (2-3.4) volts; logical "0" — + (0-0.8) volts.

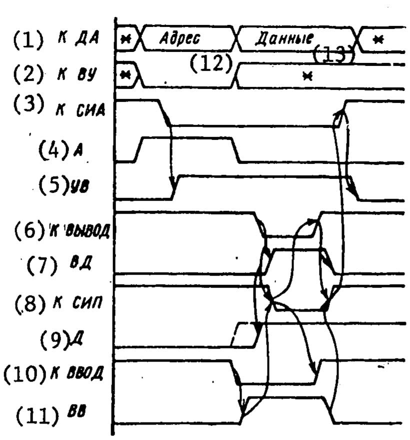
The data and state registers are built with K155IR13 elements. The data register is designed to store 16-bit words of data received from the microcomputer and to output it through the coupling buffer to external units. It may be loaded and read by program. The state register has 16 bit positions: eight low-order bits are allocated for storage of interrupt authorizations from external units and may be loaded and read by programs; the eight higher-order bits may only be read by program and serve as external unit flags.

The decoder analyzes the address part of the cycle of data exchange with the microcomputer. The bit positions 00-2 of the address together with control signals of the computer are used to produce internal and external control signals; positions 11 and 12 are used for addressing the appropriate exchange units, and positions 03-10 are used for addressing to external units connected to the particular exchange units.

The logical part of the interrupt is made with a K589IK14 element and is designed to receive eight interrupt requests from external units and organize priority service for them based on control signals from the microcomputer.

The multiplexor provides feeding of four types of information to the microcomputer: addresses of interrupt vectors; data from the state register, external units, and the content of the data register.

Figure 2 below presents a combined time diagram of the work of the exchange unit in the data input-output mode.



Key:
- (1) Channel Signal for Transmission of Data/Address;
- (2) Channel Signal for Selection of External Unit;
- (3) Channel Signal for Synchronization of Active Device;
- (4) Address Line Signal;
- (5) Address Strobing Signal;
- (6) Channel Signal of Data Output;
- (7) Strobing Signal of Transmitted Data;
- (8) Channel Signal of Synchronization of Passive Unit;
- (9) Data Transmission Signal;
- (10) Channel Signal of Data Input;
- (11) Strobing Signal of Data Received;
- (12) Address;
- (13) Data.

Figure 2. Combined Time Diagram of the Work of the Unit in Input-Output Modes.

In design terms the exchange unit is a single printed plate with dimensions 240 x 280 x 12 millimeters. It receives power from a power supply source with a voltage of +5 volts ±5 percent. The current used by the device does not exceed 1.5 amps.

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CONTROLLER FOR CONNECTION OF THE ELEKTRONIKA T3-16 KEYBOARD COMPUTER WITH THE CAMAC CRATE

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 15-19

[Article by A. M. Shcherbachenko and Yu. I, Yurlov, Novosibirsk)

[Excerpts] Electronic keyboard computers are finding ever-wider application in the automation of processes of measurement and control. They permit creating and later developing inexpensive and simple-to-operate systems for data collection and processing and for the control of various technological processes.

The low cost, simplicity of programming and introduction of the working program and the possibility of operating with words with large digit capacity make it preferable to use specialized keyboard computers in such systems in cases where the latter do not need the speed and storage possibilities of minicomputers or for economic considerations the development of systems does not allow expenditures connected with the application of minicomputers.

Proposed in this article is one of the approaches to the construction of a crate-controller, intended for the inclusion of specialized "Elektronika T3-16 (T3-16M)" keyboard computers [1] in systems for data collection and processing and control corresponding to CAMAC principles [2].

The crate-controller developed in the Institute of Automation and Electrometry, Siberian Department, USSR Academy of Sciences assures the formation and performance of CAMAC instructions in modules of a single crate; transmission of numerical information from one CAMAC module to another without being remembered in the internal registers of keyboard computers; the accomplishment of operations of tetrad output of binary numbers obtained in keyboard computers by programming; the accomplishment of interruptions according to requests from CAMAC modules.

The developed controller is used to control CAMAC modules in a precision photoplotter to record synthesized optical elements with axial symmetry, controlled from an "Elektronika T3-16M" keyboard computer [3].

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CAMAC MODULES ORIENTED TOWARD THE CREATION OF TERMINAL COMPLEXES FOR VARIOUS PURPOSES

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 20-24

[Article by Ye. N. Bobrov, V. A. Slepnev and B. V. Fesenko, Novosibirsk]

[Excerpts] At present work is being widely done on the creation of computer networks which combine a large number of territorially dispersed terminal complexes. The terminal complexes provide convenient and effective access to the computer system and permit realizing multilevel computation procedures and maximally satisfying requests of users.

In the NP [unidentified] Special Design Bureau, Siberian Department, USSR Academy of Sciences a number of modules have been developed that are intended for the organization of terminal complexes of the network of the Shared Multicomputer Center, Siberian Department, USSR Academy of Sciences. The modules were executed in the CAMAC standard, which provides the possibility of programmed control of any unit of the terminal network. Below are described the basic modules of the terminal complexes, provisionally broken down into two groups: modules for coupling a crate with different kinds of terminals and modules for coupling the crate main line with successive communication channels.

All these modules have standard control from the crate main line.

The following apply to modules of group I:

The V-340 drive serves to match the signals of the parallel interface of the "Videoton340" alphanumeric display with signals of the crate main line. The module has a width of 1 M.

The FS-1501 drive is intended for matching FS-1501 photoreader signals with crate main-line signals. The module has a width of 1 M.

The PL-150 drive matches Pl-150 tape punch signals with crate main-line signals. The module has a width of 1 M.

The V-343 drive serves for matching signals of the "Videoton-343" line printer with crate main-line signals. The module has a width of 1 M.

The UVVK-601 drive is used to match signals of the input device from UVVK-601 punched cards with crate main-line signals. The module has a width of 2 M.

The C-260 drive is intended for matching signals of the "Consul-260" electrical typewriter with crate main-line signals. The module has a width of 2 M.

The ASR-33/V-340 drive serves for the matching of ASR-33 teletype signals or of "Videcton-340" alphanumeric display interface signals with crate main-line signals. The module has a width of 1 M.

A model of a dialog-package terminal complex is being experimentally operated on communication channels with the M-6000 and BESM-6 computers.

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MICROEQUIPMENT FOR USE IN SMALL DIGITAL SYSTEMS DESCRIBED

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980 p 29

[Article by engineers V. T. Yermolov and G. E. Vasarin'sh and Candidate of Technical Sciences A. A. Chipa: "Set of Microequipment Based on a Series K580 Microprocessor"]

[Text] The Institute of Electronics and Computer Technology of Academy of Sciences Latvian SSR has developed a set of microequipment based on the K580 microprocessor for building comparatively small digital systems based on microprocessors (see Figure 1 below). It consists of two printed plates.

Figure 1

One is a single-plate microcomputer and the second is a control console (keyboard and display) and may be connected to the first by cable. A resident monitor with a read-only memory of 1,000 bytes on a microcomputer plate has been developed as system software.

The set is designed to provide developers of small digital systems based on microprocessors with inexpensive built-in microcomputers for use as design modules; to devise an inexpensive and easily mastered system of debugging programs written in the machine code of the series K580 microprocessor without using scarce standard input-output units; to develop an easy-to-handle set of training equipment for studying microprocessor technology.

Figure 2 below shows a structural diagram of a microcomputer whose central element is an eight-bit K580 microprocessor. The two-phase synchronization signals necessary for the work of the microprocessor are issued by a cyclical pulse generator built with K155 microcircuits and 2T608 transistors.

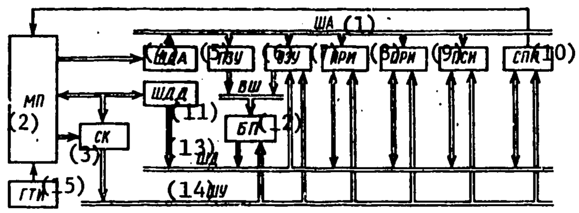


Figure 2

Key:
(1) Address Line;
(2) Microprocessor;
(3) System Monitor;
(4) Address Line Driver;
(5) Read-Only Memory;
(6) Internal Memory;
(7) Parallel Interface;
(8) Parallel Interface;
(9) Sequential Interface;
(10) Priority Interrupt System;
(11) Data Line Driver;
(12) Buffer Memory;
(13) Data Line;
(14) Control Line;
(15) Cyclical Pulse Generator.

The appropriate series 589 microcircuits are used as address and data line drivers, while the system monitor is made from a series K589 multimode buffer register and series K155 microcircuits. The monitor forms all necessary microcomputer control signals and the control line. The read-only memory unit is constructed from K505 reprogrammable large integrated circuits.

The internal memory unit is made from K565 series large integrated circuits. The outputs of the read-only and internal memory units form the auxiliary line, which is connected with the system data line through the buffer memory built with series K589 MBR's [expansion unknown].

The microcomputer has parallel and sequential interfaces for coupling with external equipment; for this the appropriate K580 series large integrated circuits are used. The microcomputer contains a system of priority interrupts. One vector of the system is used for efficient operation of the system monitor.

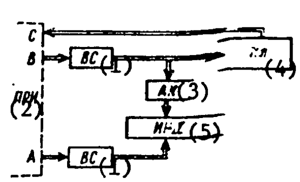
The system lines are connected to a separate plug of the microcomputer plate, which makes it possible for the user to expand the system if necessary.

Technical Description of the Microcomputer

Programming Language	Machine Codes (in 16-Position Systems)
Central Processor	K580IK80 Single-Crystal
Bit Configuration in Binary Bits	8
Speed in Operations per Second	2,600 (R-R Format)
Interrupt System	Priority, 8 Vectors
Capacity in Bytes:	
Internal Memory	1,000
Read-Only Memory	2,000
Number of Programmable Input-Output Lines:	
Parallel	48
Sequential	1
Voltage Supply from DC Network, in volts	+5, -5, +12, -12
Dimensions, millimeters	280 x 240

When system software is used a control console made of an individual plate with a button-type keyboard and one-line display is connected to the microcomputer plate. The keyboard buttons are broken into two groups. One has 16 buttons and is designed for the set of 16-bit codes (0÷F); the other is formed of eight buttons and is for executing monitor commands.

The one-line display can show six 16-bit characters and is assembled from seven-segment light-emitting diodes. The keyboard and display are served by the system monitor using one of the parallel interfaces of the microcomputer. In this case the code is outputted through port A of the interface to segments of the display (see Figure 3), while the excitation code of the lines of the matrix of the keyboard and anode switches goes through port B. The code taken from the columns of the keyboard matrix is fed to the microcomputer through port C. The MOS outputs of ports A and B are coupled to the console circuit through a group of series K155 TTL [expansion unknown] gates. The console has dimensions of 240 x 140 millimeters.



Key: (1) Gates;
(2) Parallel Interface;
(3) Anode Keys;
(4) Keyboard;
(5) Display.

Figure 3

The system monitor outputs the content of any memory address to the display with simultaneous display of the address; outputs the content of the internal registers of the microprocessor; writes new codes from the keyboard to assigned cells of the internal memory unit; launches a program from any address and stops it at five predetermined addresses; performs a program step by step; interrupts running of a program at any moment.

When the microcircuit plate is used as a specialized built-in computing unit the user can employ all 2,000 bytes of the read-only memory for his own working programs and use both parallel interfaces. In this case, however, it is not possible to use the system monitor or for the microcomputer to work together with the control console.

This set of microequipment can be recommended for building small microprocessor systems in various fields of engineering and also as a convenient and inexpensive means of learning the specifics of using microprocessors.

[72-11176]

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CSO: 1863

BASIC FEATURES OF PS-300 CONTROL COMPUTING COMPLEX ADVERTISED

Moscow VYCHISLITEL'NYYE SREDSTVA V TEKHNIKE I SISTEMAKH SVYAZI in Russian No 5, 1980, on back cover

[Advertisement: "The PS-300 Control Computing Complex"]

[Text] The PS-300 CCC [Control Computing Complex] is designed for use in automated control systems for local industrial processes, in information-measurement systems for direct digital control, and at the lowest hierarchical level of complex hierarchical systems.

Composition of the Basic PS-300 Set with PS-300 Computer

Command System	variable, expandable
Equivalent Productivity, ops/second	50,000
Main Memory Volume, bytes	20,000
Number of External Units Connectable	12
Linkage	2K
Model Types	instrument, stand
Dimensions, millimeters	266 x 483 x 585

-- FS-1501 Photoreader or Cassette Store

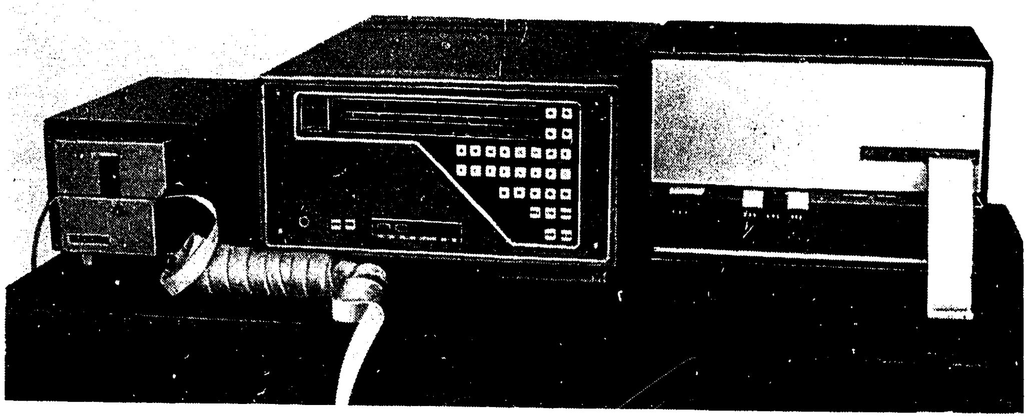
-- MT-1016 Printer

-- Analog Signal Input Unit with Galvanic Separation and up to 32 Connectable Channels

-- Discrete Signal Input Unit with up to 128 Connectable Channels

-- Analog and Discrete Signal Output Units with up to 16 and 128 Analog and Discrete Channels Respectively

The PS-300 CCC performs collection and primary processing of data, monitoring and registration of parameters, output of information on the course of



The PS-300 CCC

the industrial process to the operator, calculation and output of control actions, and calculation of technical-economic indicators.

A magnetic tape cassette store can be used for external memory and the input unit.

The software includes packages of applied programs, including dynamic optimization of industrial processes; for automated control systems of continuous industrial processes that monitor power industry facilities and control them; programs and methodological means for systems of discrete control of flow lines; a computer program for a multichannel substance analyzer; a general-purpose system of adaptive control of industrial facilities, and others.

The basic set costs 51,000 rubles.

The PS-300 CCC is manufactured by the Tbilisi Experimental Control Computing Machine Plant of the Elva Science-Production Association (380086, Tbilisi, Dzhikiya Street, 10).

Orders for the PS-300 CCC and its delivery are made through the Soyuzsistemkomplekt Trust (103001, Moscow, Malaya Bronnaya, 28/2).

[72-11176]

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APPROVED FOR RELEASE: 2007/02/08: CIA-RDP82-00850R000300100033-1

UDC 681.3

PS-300 CONTROL COMPUTING COMPLEX DESCRIBED

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980 pp 6-8

[Article by Deputy General Director of the Tbilisi Science-Production Association Elva and Candidate of Technical Sciences D. A. Todau and engineers N. A. Barbakadze, N. G. Sokhiya, U. N. Devdariana, D. A. Shekriladze, and S. I. Yakubov: "Controlling Computer Complex Based on the PS-300 Computer"]

[Text] The controlling computer complex based on the PS-300 computer (the PS-300 CCC) is designed for use in automated control systems for local industrial processes and aggregate units, in systems for scientific experiments, monitoring and diagnosis, information and information-measurement systems, and at the lowest level of the hierarchy of complex hierarchical control systems.

The PS-300 CCC is composed of units with self-sufficient power supply that are complete in terms of function and design. They can be arranged on standard frames, tables, and racks. No additional work is required in this case to calculate and install the power supply.

The units included in the PS-300 CCC are outstanding for high error-detection and low power input thanks to the use of integrated microcircuits with DMDP [expansion unknown] structure (series 176). They have a highly developed monitoring and diagnosis system which improves the reliability of data collection, processing, and representation.

The PS-300 CCC performs the following basic functions:

a. collection and initial processing of data from sensing units;

b. representation of data on digital console instrument at operator request;

c. continuous representation of data on digital instruments with cyclical updating;

d. signaling deviation of parameters from norms;

e. feeding constant values from the console;

f. connecting the requested program from the console for execution in the processor;

g. disconnecting the requested programs;

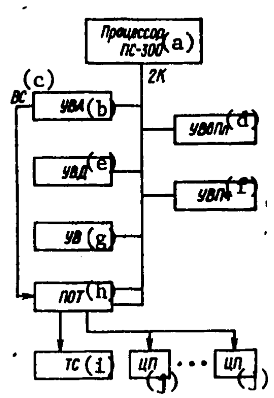
h. data processing in real time;

i. outputting control actions;

j. transmitting data to higher-level computers.

Composition of the PS-300 CCC

Figure 1 below gives a structural diagram of the base model of the PS-300 CCC.



Key: (a) PS-300 Processor;
(b) Analog Signal Input Unit;
(c) Internal Linkage;
(d) Output to Punched Tape;
(e) Discrete Signal Input Unit;
(f) Output to Printer;
(g) Output Unit;
(h) Operator Console;
(i) Deviation Warning Panel;
(j) Digital Instruments.

Figure 1

The base set of the PS-300 CCC (see Figure 2 below) includes a PS-300 computer, a linkage unit to the object, and equipment for exchange of information between the operator and the units of the complex. The PS-300 computer consists of a PS-300 processor, a punched tape input unit, and a printer output unit. The unit for linkage with the object also includes an analog signal input unit, a discrete signal input unit, and an output unit. Equipment for information exchange between the operator and the units of the complex includes the operator's console, the deviation warning panel, and the digital instruments.

All the units of the PS-300 CCC have outlets to a standard 2K coupling. The PS-300 CCC envisions internal linkage to connect the analog signal input and operator's console units.

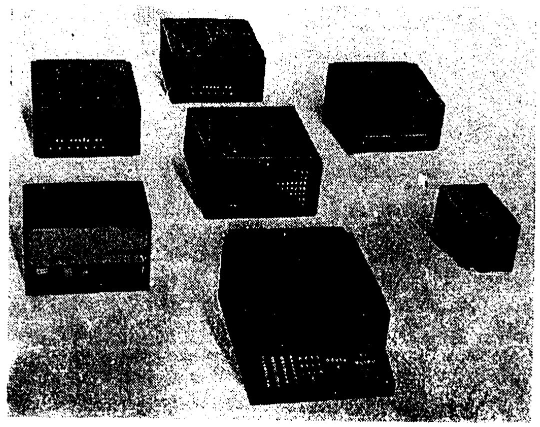


Figure 2

The interrupt system in the PS-300 computer is a priority circuit system with one level; the sources of interruption are programs, the timer, and external units.

Punched tape is fed by a FS-1501 unit. Output is printed using a small MPU16-3 printer

Detailed information on the PS-300 computer has been published at an earlier time.*

Basic Technical Description of the PS-300 Computer

Volume of Main Memory, in bytes	20,000
Equivalent Productivity in Short Operations per Second .	50,000
Volume of Decision Field in Cells of Similar Structure .	24 x 16
Number of Outlets to 2K Linkage	12

The Analog Signal Input Unit

This unit is designed to handle data from analog signal pickups: switching, normalization, conversion to binary code, and output into the processor and operator's console. The unit has contactless switching with galvanic isolation of the input circuits.

*Prangishvili, I. V., Todau, D. A., Abramova, N. A., Vepkhvadze, A. N., et al, "The PS-300 Computer," PRIBORY I SISTEMY UPRAVLENIYA No 10, 1978.

Basic Technical Description of the Analog Signal Input Unit

Number of Input Channels	32
Value of Signal:	
Input, in milliamps	0-5
Output, in binary bits	10
Basic Calculated Error, %	0.25
Conversion Frequency, in Khz	5
Input Impedance of Measurement Channel without Norming Resistor, in Kohm	50
Coefficient of Suppression of Noise Signal, in dbs:	
Transverse Frequency of 50 Hz, at least	60
Longitudinal Frequency, at least	100
Maximum Distance to Pickups, meters	500
Power Input, watts	25
Dimensions, millimeters	482 x 482 x 265

Discrete Signal Input Unit

This unit is used to switch and transmit to the processor data from initiative and noninitiative pickups of discrete signals. The input circuits of this unit are protected against accidental voltages of 220 volts relative to the ground in the linkage line with the "dry contact" sensors. The unit also has automatic monitoring of the linkage line with the sensors for a break in the circuit or a short circuit to the ground.

Data is fed to the processor by groups. The interrupt signal goes to the processor when the state of the initiative pickups changes from "0" to "1," from "1" to "0," and for any change. Along with the interrupt signal the unit issues to the processor an address and information on the sensors of the group in which the change occurred.

Discrete signal pickups of the "dry contact" type and two-position pulse type with signals of 2.4-5.25 and 0-0.4 volts, corresponding to logical "1" and "0" respectively, are connected to the discrete signal input unit.

Basic Technical Description of Discrete Signal Input Unit

Number of:	
Two-Position Inputs	128*
Sensors in a Group	8
Frequency of Polling of Sensors, Khz	10
Maximum Distance to Sensors, meters	500
Power Input, watts	25
Dimensions, millimeters	482 x 482 x 265

*The number of initiative sensors is unlimited.

In the analog and discrete signal input units cyclical polling of connected sensors is organized with writing of results in the buffer memories of these units. When the processor refers to the analog or discrete signal input unit the information is outputted from the internal memory and, thus, the frequency of data exchange between them and the processor in fact depends entirely on the frequency of the programmed processor channel.

With the exception of the channel switching blocks the diagrams of the analog and discrete signal input units are identical. This kind of standardization greatly simplifies their manufacture and use.

Output Unit

This unit is designed to output analog and discrete signals to influence the controlled object. It receives the address of the channel and the value of the action in binary code from the processor and converts the analog action into a standardized current signal or amplifies the discrete action signals. It is possible to assign values of analog and discrete action signals in binary code by manual means from the engineer's console. They are given in groups.

Basic Technical Description of the Output Unit

Number of Channels for Outputting Analog Action	16
Output Analog Signal, milliamps	0-5
Load Impedance, in Kohm, not more than	2.5
Error in Processing Analog Action Signals, %	0.25
Conversion Time, milliseconds	5
Number of Channels:	
Two-Position Action	128
In a Group	8
Parameters of Two-Position Action:	
For Logical "1"	24
For Logical "0"	1
Maximum Distance from Output Unit to Regulators and Actuating Mechanisms, meters	500
Power Input, watts	25
Dimensions, millimeters	482 x 482 x 265

Operator's Console

The functions of the operator's console include indicating the values of parameters being measured and calculated on the digital instrument, connecting a requested program in the line for execution in the processor or removing a program from the line, feeding the values of constants to the processor, and indicating the state of the particular units of the PS-300 CCC.

The console is connected to the processor by two interface cards, one of which is designed to connect the processor to the unit for controlling external digital units and the deviation warning panel. This unit is designed for inclusion in the console and provides output of information from the processor and the analog signal input unit on the external digital instruments as well as warnings on the warning panel when parameters deviate from the norm. The external digital instruments and deviation warning panels can be put on mnemonic diagrams or at any place convenient for the operator.

Basic Technical Description of Operator's Console

Bit Configuration of Digital Instruments in Decimal Bits	4
Maximum Number of:	
Analog Signal Input Units Connected	4
Digital Instrument	32
Parameters Output to Signal Panels	32
Power Input, watts	60
Dimensions, millimeters	482 x 482 x 265

Software of the PS-300 CCC

The software of the PS-300 CCC includes a system of commands, a library of commands (arrays of adjustment information), and the following systems: control; input-output control (drivers); test; translation-simulation, and command design. The programs of the translation-simulation and command design systems and the library of operators form the cross-software of the PS-300 CCC. The bulk of it is written in FORTRAN-IV; it has been written for the YeS disk operations system and the ASVT [possibly modular system of computer equipment] disk operations system.

The PS-300 CCC is supplied with a package of applied programs. The first phase of the applied software of the PS-300 CCC contains the following packages: standard programs and programs for adaptive control oriented to automated control systems or chemical production; monitoring and control of power industry facilities; analysis of the composition of matter; processing of chromatographic data; dynamic optimization of industrial processes; system of discrete control of flow lines.

Characteristics of the PS-300 CCC

The central computer in the PS-300 CCC is a computer with rearrangeable homogeneous structures. The presence of an arithmetic-logical unit with rearrangeable homogeneous structures in the PS-300 processor makes it possible to feed new commands that are essential to the user to the command system without changing the machine circuits. Although machines with microprogram control also have this advantage, when the same commands are repeated in computers with microprogram control the corresponding microprogram is run each time, whereas in the PS-300 computer the homogeneous medium, once adjusted, guarantees subsequent hardware execution of these commands.

The cross-software for translation and simulation makes it possible to debug new programs without disconnecting the control computing complex for a long time.

The internal linkage insures continuous representation and updating of data from the analog signal sensors in the digital instruments even if the processor malfunctions. This is especially important for normal maintenance of an industrial process when switching to manual control. It greatly improves the reliability of a control system built on the basis of the PS-300 CCC.

The reliability, noise suppression, and speed of analog signal input are improved through the use of contactless switching and galvanic isolation of the input analog channels.

The functional and design completeness of all the units of the PS-300 CCC, which is expressed in the fact that all the elements necessary to accomplish consolidated functions are contained in one invariable design, simplifies assembly for designing automated control systems for industrial processes or other systems as well as the ordering and manufacture of control computing complexes.

[72-1176]

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CSO: 1863

HYBRID COMPUTERS

SPECIALIZED HYBRID CONTROL COMPUTERS

Moscow SPETSIALIZIROVANNYYE GIBRIDNYYE UPRAVLYAYUSHCHE-VYCHISLITEL'NYYE USTROYSTVA in Russian 1980 (signed to press 6 May 80) pp 284-286, 288

[Table of contents and annotation from book "Specialized Hybrid Control Computers", by Kemer Borisovich Norkin, Izdatel'stvo "Energiya", 5,500 copies, 288 pages]

Contents Page

The problems of constructing specialized and problem-oriented hybrid computers are considered and the methods of describing the machines and programs, the principles of controlling the calculating process and methods of displaying digital variables are given.

Intended for developers of various types of computer equipment. It will be useful to students and graduate students specializing in the field of computer technology.

[108-6521]

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CSO: 1863

DEVELOPMENT OF SPECIALIZED HYBRID CONTROL COMPUTERS

Moscow SPETSIALIZIROVANNYYE GIBRIDNYYE UPRAVLYAYUSHCHE-VYCHISLITEL'NYYE USTROYSTVA in Russian 1980 (signed to press 6 May 80) pp 5-16

[Foreword and introduction from book "Specialized Hybrid Control Computers", by Kemer Borisovich Norkin, Izdatel'stvo "Energiya", 5,500 copies, 288 pages]

[Text] Foreword

The proposed book is addressed to specialists whose activity is related to development of specialized control computer equipment. This has in mind both those who directly make specific engineering decisions and those who are responsible for planning the system as a whole and its configuration and those who conduct theoretical investigations in this field.

Hybrid control computer devices are considered in the book. This does not mean that the use of hybrid devices is recommended in all cases. However, it is obvious that only on the basis of the theory of hybrid computer systems can specific realizations of control computer devices be achieved with different ratio of analog and digital variables--from completely digital to completely analog. Thus, selection of the optimum ratio of the volumes of analog and digital variables and specifically selection of the point of conversion of analog variables to digital form is carried over from the sphere of scholastic a priori discussions to the sphere of precise calculations. Purely digital or purely analog approaches do not provide this capability.

The main thing that distinguishes the ideology of constructing computer devices being developed in the given book is the viewpoint that the form of information display (analog or digital) is not, regardless of how paradoxical it seems, the main feature by which digital and analog computers of traditional configuration are distinguished. The determining factor is the difference in the degree of automation, algorithmization and parallellism of the calculating process. Indeed, the variety of possible engineering solutions in the field of display of variables is now so great that it is obviously rational to first determine the configuration of the system and its operating program and then to determine the optimum form of information display in its different parts from economic and other concepts. Thus, we feel that it is incorrect to reject the digital or analog method of information display without consideration of the specific situation in which the corresponding computer system is being developed. This means, according to the adopted method of synthesis, that the initial structure must be hybrid so that a purely digital, purely analog or some other intermediate solution could be found during optimization from this structure.

The structure of some universal hybrid computer oriented toward a very broad class of problems is proposed in the book to realize the indicated useful property of the hybrid approach. The structure has great flexibility, i.e., it permits one to find many possible variants of technical realizations. Many generally accepted engineering solutions are also found as a special case. The variety of permissible variants provides the possibility of optimization.

The plan of the proposed book is simple. It is divided into four parts by content. The language of describing the iteration processes and machines, the structure of a universal iteration machine and methods of realizing the individual devices of it are given in Part 3. The developed formalism requires justification both in the sense of feasibility and in the sense of practical realizability of the recommendations ensuing from it. Therefore, general principles are given in Part 1 which should be the basis of efficient hybrid systems, while principles of engineering realization of devices of iterative hybrid machines are given in Part 2. Part 4--the largest in the volume--is devoted to applied aspects of the developed methods. Examples of formalized synthesis are given here and examples of synthesis of specific devices are presented. Moreover, a number of specialized machines which embody the principles recommended in the book are given in Part 4.

A. A. Fel'dbaum and L. N. Fitsner were innovators of investigations in the given direction in 1959. Many authors influenced the formation of views outlined in the book. This is indicated by the bibliography. I would especially like to note the influence of such well-known scientists as G. Ye. Pukhov, A. V. Kalyayev, B. Ya. Kogan and R. G. Smolov. I am glad to note the important assistance which Ye. G. Aleksandrov, S. A. Vazhnov, S. B. Kleybanov, N. L. Logunova, E. D. Mit'kov, I. P. Myshkin, V. M. Prut, V. D. Spiridonov, O. B. Suslova, G. G. Kharchenkov, A. B. Shubin and I. S. Yakovlev provided in development and constructive criticism of the outlined ideas.

Introduction

An attempt is made in the book to develop and universally justify an approach to construction of hybrid computer systems which would make it possible to create specialized control computer devices with different degree of hybridization--from almost totally digital (for example, on microprocessors) to purely analog--as a function of conditions of application.

The word hybrid is understood in the generally accepted meaning: processing of digital and continuous (analog)* variables is possible in the systems under consideration. The word specialized is interpreted very broadly. It is assumed that a universal machine may be only an abstract or theoretical machine, while practically any specific machine is specialized to one degree or another. In order to talk about different degrees of specialization, narrowly specialized devices of the regulator type, the simplest computers, filter, signaling devices, optimizing devices and so on and broadly specialized devices of the problems-oriented computer type, for example, are considered.

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*The word continuous is better than analog in our view, since it is frequently impossible to see any "analogy" whatever in analog variables. Following tradition, we frequently used the term analog.

The conviction of the timeliness of new research on hybrid computer devices developed because the following propositions are sufficiently reliable:

1. Non-automated systems with purely analog display of variables do not have any serious future prospects.

2. It will never be possible in the future to construct control computer systems based on digital principles alone--there will always be the need to receive some input data and to issue the results in analog form.

3. The point of converting data from analog to digital form and from digital to analog form in future systems will be flexible as a function of the specific problems and significant volumes of calculations may be required for data processing in analog form.

4. The existing ratio between the distribution of digital and hybrid systems (with favor given to digital systems) is explained only by the historically established insufficient automation of early analog processors and will vary sharply in the future under the influence of success in automation of hybrid systems in favor of expanding the application of these systems.

5. Data processing using significant volumes of continual variables will be related to finding complex phase trajectories of dynamic systems and functionals of sets of these trajectories and to organization of procedures of purposeful selection of the parameters which determine these trajectories.

6. Future hybrid systems will be developed not only as a combination of analog and digital parts but as a unit whole as well.

7. Future systems will combine high autonomy with the possibility of using them as peripheral equipment of large digital systems of the most varied configuration.

The investigations, the results of which are outlined in the book, were stimulated by analyses and also mainly by the following factors.

First, there was the conviction as a result of prolonged practical work in the field of computer technology that the nomenclature of possible engineering solutions at the disposal of specialists was too sparse and does not correspond to modern ideology, engineering and technology. Because of this, many "generally accepted" solutions are only a special extreme value found in this "sparse" set. If the variety of versions is expanded, one can achieve an appreciable advantage due to better adaptation of designs to specific problems. The time has now come when the range of versions can be expanded due to the new structures which utilize the latest advances of engineering and technology.

First, the fundamental incorrect idea of the ratio of the capabilities of analog and digital principles of constructing computer equipment caused specific concern. And there still exists the opinion that analog devices are less expensive, have insurmountably limited accuracy, high speed and weak logic capabilities and are incapable of algorithmic calculations. Digital devices are more expensive and slower but have unlimited accuracy, unlimited logic capabilities and easily carry out algorithmic calculations. More detailed analysis partially presented in the proposed book showed that the enumerated properties are more inherent to configurations in which analog or digital components were traditionally used rather than to the method of information display. Let us give just one example. As is known, development of so-called structural-analog digital devices is now possible. Digital versions of all the analog blocks can be taken as the resolving elements of these devices. The variables in structural-analog digital machines are a parallell binary code. Combinations of resolving elements are carried out, as in analog machines, but by multistrand conductors (the number of strands is equal to the number of digits of the binary display). If a configuration traditional to analog computers is taken, there will be neither algorithmic nor broad logic capabilities in this purely digital device. Colossal effective speed will then be achieved. It is now time to synthesize control computer devices from unified configurational aspects without regard to the form of display of variables, while the form of the display is selected, for example, from economic concepts. It is now known at the modern stage how to diversify the methods of display of variables.

Third, the generally accepted rules of interaction of digital machines and hybrid peripherals do not correspond to the problem of coordinated use of the capabilities of both types of computer devices. A hybrid peripheral usually has a too strong negative effect on the central digital computer in the traditional structure. On the other hand, cases when the digital computer is used with insufficient efficiency comprised the majority among all cases of access of the hybrid peripheral to the digital computer. All operations on servicing these accesses can be carried out completely by elementary hardware. There is a need to improve the rules of interaction of digital computers with hybrid peripherals, to give greater autonomy to the hybrid part and to resort to digital computers only in those cases when use of them is effective.

And finally, the inveterate intuitive method of synthesis of hybrid control computer systems is archaic at the modern stage. Not only specific systems are developed in this case without any formal apparatus, but even many new proposals are formulated in terms of the operating principle. The time has come when the first approximation of the general theory of hybrid computers and the first approximation of the formalized method of synthesis can be formulated. And even if this method is unperfected initially and labor expenditures on synthesis are not reduced completely or are reduced insignificantly, one should still move along the path of formalized synthesis since only this type of synthesis permitted a flexible response to the needs of practice in all other fields of technology.

The indicated difficulties and deficiencies are overcome by the nontraditional approach to the problem of constructing specialized hybrid devices. A very flexible structure of a universal hybrid machine oriented toward the most diverse parametric problems for differential equations solved by iteration methods is proposed. The proposal is based on some innovations in the field of the component base, methods of display of variables, methods of controlling the calculating process and method of describing machines and programs. The practice of using this structure for different applications shows that it is easily adapted to different conditions of application. It provides variety and economy of methods of displaying analog and digital variables and if necessary a high level of automation of the calculating process, algorithmization, significant autonomy (up to separability) during operation in hierarchical systems and a number of other useful properties.

The development of the general theory of hybrid computer devices is essentially discussed in the book, but significant restrictions of generality and strictness must be permitted in some problems.

First, the class of problems is limited and primarily problems consisting of multiple solution of ordinary differential equations, formulation of functionals from sets of solutions of these equations and organization of processes of selecting the parameters in these equations with regard to the purpose of selection and the past values of derived functionals are considered. These very widespread and rather universal problems are briefly called iteration problems over parameters of differential equations or simply iteration problems. Such concepts as differential equation, set of solutions, parametric set of solutions, phase coordinate, phase trajectories, functional and operator are assumed to be known.

Second, a number of terms not strictly defined is used. The greater part of them are generally accepted in computer technology. These are primarily general concepts: input, output, computer, analog computer, digital computer, variable, variable value and so on. A number of concepts must be borrowed from the theory of formalized synthesis of logic devices. Some concepts are introduced without strict definitions, being oriented toward the semantics of the corresponding words. Let us enumerate the most important of these concepts.

An elementary machine is the smallest hybrid machine which can rationally be regarded as a unified whole. The volume of the machine is the maximum dimensions of the problem being solved and the maximum number of variables used in the problem. The capacity of the machine is the maximum rate of variation of phase coordinates and some analog of the concept of effective speed. The computer product is the concept that characterizes the reason the machine is developed and connected. One can assume that the product of a computer is some process or some sequence of values at the outputs of special or specially noted components of the machine.

Besides those enumerated, other strictly undefined concepts are found in the book which are essentially explained only by their properties during outlining.

An finally, the level of the strictness of exposition is largely inferior, for example, to the level of strictness of the theory of finite automatons. This was inevitable at the stage of formation of theory.

Let us explain briefly why the range of problems being solved is limited to iteration problems over parameters of differential equations. Iteration processes, understood as processes of multiple application of some operation to its result, are very frequently accomplished by computer equipment. This is explained by the fact that the highest efficiency is achieved with homogeneous calculations. As a result direct calculation (without the iterative process) is less advantageous, although the iteration process may even include a much greater number of operations. The effectiveness of using iteration processes increases especially with respect to parallel calculations. Actually, the high degree of parallellism of computer devices causes large expenditures for initial input of the problem. It is obvious that single use of the system after input of the problem is not advantageous. Hence ensues the feasibility of orientation toward iterative calculation processes and especially toward iterative processes related to differential equations, since in the latter case the effectiveness of parallel calculations increases even more.

If the process of developing computer equipment is analyzed, it must be stated that the main difficulty is understanding and description of the machine as a whole, including its configuration and operating process. This difficulty is aggravated by the fact that machines are developed as a result of the work of collectives, frequently rather large collectives, rather than individual specialists. The only method of clear description of complex systems is sequential decomposition of the description. Confining ourselves to the given method, let us present for a beginning the most general description of the working process of an automated hybrid computer system.

A hybrid system is designed to convert input data and external synchronous signals to other variables which are actually its product. Conversion is accomplished by the resolving elements connected to a special network. The input data and the conversion program are stored in a special memory or are assigned by the position of different machine control members. The lifetime of a hybrid system is assumed to be divisible by the periods of the initial position, operation and shutdown. Machine operation consists in the following. Different machine control members are set to the required initial position, while a special memory is filled with the necessary contents. The position of the control members and the content of the memory are called adjustments. The adjustments are set directly manually, manually through the input device or automatically through the readout device or from devices of the upper level of hierarchy. Further, the machine is transferred to the "Operation" mode if necessary and begins to change its states automatically (information variables, phase coordinates and values of output and internal variables) according to adjustments in time by digital or analog means and automatic exchange of information is accomplished inside the machine and with the external environment. According to the meaning of the concept product indicated above, the machine product is the values of certain variables at certain intervals or at certain moments of the operating period. Shutdown provided by the program or caused by the external environment (operator or an old machine) can begin during operation. No variables change in a hybrid machine during shutdown that are equivalent to stopping of time.

A period of the initial position or operation may begin after shutdown. By definition, adjustments can be changed only during periods of the initial position. The unit of work is the problem, i.e., the entire product between two variations of adjustments.

The functions of each resolving element of a hybrid system change form more or less strongly due to the effect of adjustments and special control variables. By definition, control variables change during operating periods. Thus, the variable functions of resolving elements may occur during periods of operation and the initial position.

An automated communications system between components function in the general case in a hybrid system. Methods of combining the components and parameters of communications channels are determined by the adjustement and control variables. The control and information variables may occur outside the system, but they are primarily formed inside it. Therefore, separation of variables into control and information is arbitrary and serves to facilitate understanding and description of machines and their components. One or another type of variables can be formed on a unified basis and the type of variable can be converted by using the operation of conferment. This will be discussed in more detail below.

The given external description of a hybrid system with details permits a considerable variety of versions that corresponds to practical needs. Since hybrid devices are more efficient as problem-oriented and specialized devices, this leads to the need to have a significant nomenclature of them. Moreover, the decision to use universal computers is made in many cases only because development of a specialized device, even one known to be inexpensive, is itself unjustifiably laborious to the developer. The timeliness of developing methods of synthesis of specialized hybrid devices is obvious in this situation. Therefore, a significant part of the book is devoted to the problem of synthesis.

The traditional methodology of synthesis has been adopted. Its essence is that some standard, universal structure has been adopted as the basis. Everything that is not required for working with the given flow of problems is thrown out of this structure and equivalent transformations of the remainder are made to optimize some, for example, economical criterion.

An obvious weak point of this method is the dependence of the final result on the initial structure. However, no methods of synthesizing an optimum structure have yet been found, so this method is inevitable. In order to lessen the effect of this deficiency, one can select all the known structural proposals with regard to the state of the art at the moment the development is introduced. This is not such a difficult problem. First, there are not so many developed and complete proposals on the structures of hybrid systems. Second, it is frequently not required to bring the synthesis to a final conclusion to analyze the quality of the engineering solutions. Third, it is rare that the same designer or organization synthesizes specialized devices for very many fields of application. Making the area of applications more specific usually permits one to select a single baseline structure after several attempts at least until there is a fundamental change in the technology of the resolving element.

[108-6521]

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PRACTICAL SYNTHESIS OF PROBLEM-ORIENTED HYBRID DEVICES

Moscow SPETSIALIZIROVANNYYE GIBRIDNYYE UPRAVLYAYUSHCHE-VYCHISLITEL'NYYE USTROYSTVA in Russian 1980 (signed to press 6 May 80) pp 218-228

[Excerpt from chapter 11 of book "Specialized Hybrid Control Computers", by Kemer Borisovich Norkin, Izdatel'stvo "Energiya", 5,500 copies, 288 pages]

[Excerpt] 11.3. An Aircraft Navigation Computer

The problem of aircraft navigation has essentially already become a classical problem. The present position of an aircraft must be computed on a map during navigation on the basis of data of various measuring instruments, input data and data of radio beacons. These calculations are essentially simple, but they require a considerable volume of apparatus. It is of interest to consider the possibility of using the outlined methods to reduce the volume of apparatus by multiple use of components.

Table 11. 7. Input Data for Navigation

Number of Item	Notation	Measurement Range	Name
1	x_{pi}; y_{pi} $x_{p(i+1)}$; $y_{p(i+1)}$	Up to 2,000 km	Rectangular coordinates of the i-th and (i + 1)-th turning points of the route (PPM) with respect to the origin of a half-route chart (see Figure 11.10)
2	x_{mi}; y_{mi}	Up to 2,000 km	The same as item 1 for beacons (see Figure 11.10)
3	W	180-1,200 km/hr	Ground speed of aircraft with respect to ground surface
4	US	0-30°	Drift angle--angle between air (see item 5) and ground speed (see Figure 11.13)

[Table continued on following page]

Table 11.7. [Continued from preceding page]

Number of Item	Notation	Measurement Range	Name
5	V	180-1,200 km/hr	Air speed--speed of aircraft with respect to air (see Figure 11.13)
6	K	0-360°	Course--angle between longitudinal axis of aircraft and initial direction of readout (see Figure 11.13)
7	UK	0-360°	Angle of chart--angle between meridian of initial direction and mean meridian of position of half-route chart (see Figure 11.12)
8	U	0-250 km/hr	Wind speed (U_0 at initial moment, see Figure 11.3)
9	δ	0-360°	Wind direction (δ_0 at initial moment, see Figure 11.13)
10	D	0-400 km	Distance from beacon to aircraft
11	A	0-360°	Azimuth of beacon--true bearing of aircraft with respect to beacon

The input variables in aircraft navigation are those enumerated in Table 11.7. The necessary refinements can be found in [54]. The output variables used in navigation are enumerated in Table 11.8. The abbreviated names of the navigation variables are explained in Tables 11.7 and 11.8 and in Figures 11.10 to 11.13. The navigation system is an inertial type with correction by radio beacon data. The following flight modes are distinguished.

1. Shortest distance. The FPU [Actual track angle] must be maintained so that the aircraft flies toward the PPM [Turning point] all the time.

2. Correction. Accurate values of the output variables of the device are introduced from the beacon data.

3. Turning. The goal of the aircraft changes (it flies toward a new PPM).

4. Operation. Main operating mode of navigation equipment. There is partial inertial calculation of output variables.

5. Memory. The enumerated W and US are not measured; the flight is made on the basis of the nearest previous memorized values. All calculations are made inside the system.

Table 11.8. Output Variables of Aircraft Navigation Device

№ п/п (1)	(2) Обозначение	(3) Наименование
1	z_{ni}	(4) Отклонение самолета по заданной линии пути (см. рис. 11-11)
2	W_z	(5) Проекция W на отклонение z_n
3	S_i	(6) Расстояние от очередного *ППМ* (см. рис. 11-11)
4	D_i	(7) То же, что п. 3, но в режиме *Кратчайшее расстояние* (см. далее)
5	sin *ЗПУ*$_i$; cos *ЗПУ*$_i$	(8) Синус и косинус заданного путевого угла *ЗПУ* на данном участке маршрута
6	sin *ФПУ*$_i$; cos *ФПУ*$_i$	(9) То же, что п. 5, для фактического путевого угла *ФПУ* на данном участке маршрута (необходимо выдавать в режиме *Кратчайшее расстояние*, см. далее)
7	U; δ	(10) Расчетные значения скорости и направления ветра. (Эти данные выдаются только в режиме *Работа*, см. далее)
8	x_i; y_i	(11) Текущие координаты самолета в прямоугольной системе координат

Key:

1. Number of item
2. Notation
3. Name
4. Deviation of aircraft along given flight path (see Figure 11.11).
5. Projection W onto deviation z_p
6. Distance from next PPM (turning point) (see Figure 11.11)
7. The same as item 3, but in the Shortest distance mode (see below)
8. Sine and cosine of given track of ZPU [Given track angle] on given leg of route
9. The same as item 5, for actual track angle FPU on given leg of route (it must be given in the Shortest distance mode, see below)
10. Calculated values of wind speed and direction (these data are issued only in the Operation mode, see below)
11. Present coordinates of aircraft in rectangular coordinate system.

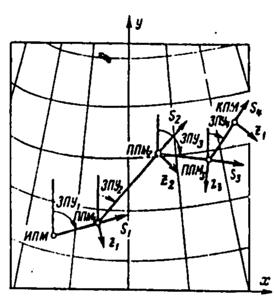

Figure 11.10. Example of Aircraft Route on Half-Route Chart

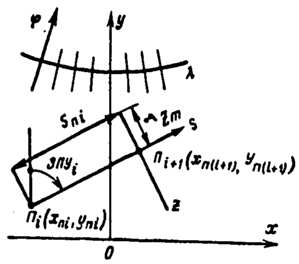

Figure 11.11. Rules for Formation of Navigation Coordinates During S-z Navigation

The adopted system is called S-z navigation. The flight takes place along the shortest curves (special geodesic lines [54]) passing through the PPM. A S-z coordinate system must be given for each leg of the flight for S-z navigation. These are rectangular coordinates. The origin is the point of the next (i + 1)-th PPM. The S-axis coincides with the line of flight and is aligned toward the i-th PPM.

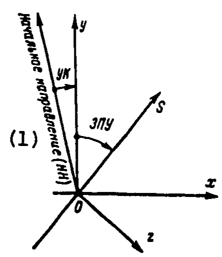

Figure 11.12. Orientation of S-z Coordinates With Respect to Half-Route Chart

Key:
1. Initial direction (nn)

Data on the PPM, the initial point of departure IPM and the final destination are given in geographic coordinates. It is assumed that the geographic coordinates of the PPM and beacons are recalculated to rectangular coordinates by using ground computers by the formulas:

$$x_i = R\Delta\lambda_i \cos\varphi_i; \tag{11.7}$$

$$y_i = R\left(\Delta\varphi_i + \frac{\Delta\lambda^2_i}{4}\sin 2\varphi_i\right), \tag{11.8}$$

where R is the earth's radius, $\Delta\lambda_i = \lambda_i - \lambda_0$, $\Delta\phi = \phi_i - \phi_0$, ϕ_i and λ_i are the latitude and longitude of the corresponding checkpoint and ϕ_0 and λ_0 are the latitude and longitude of the origin of the half-route chart.

(1)

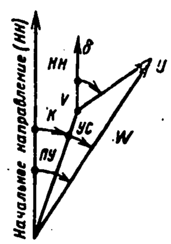

Figure 11.13. Consideration of Wind Direction and Speed

Key:
1. Initial direction (nn)

The angle of convergence (the angle between the meridian of the i-th beacon and the meridian of the origin of the half-chart route) ΔN_i for navigation calculations is determined by the formula

$$\Delta N_i = (\lambda_{Mi} - \lambda_0)\sin\frac{\varphi_{Mi} + \varphi_0}{2}. \tag{11.9}$$

The distance between adjacent PPM is calculated by the Pythagorean formula

$$S_{ni} = \sqrt{(x_{n(i+1)} - x_{ni})^2 + (y_{n(i+1)} - y_{ni})^2}, \tag{11.10}$$

while the trigonometric functions of the PZU are calculated by the formulas:

$$\sin ЗПУ_i = \frac{x_{n(i+1)} - x_{ni}}{S_{ni}}; \tag{11.11}$$

$$\cos ЗПУ_i = \frac{y_{n(i+1)} - y_{ni}}{S_{ni}}. \tag{11.12}$$

The values W, US and K are entered in the aircraft navigation computer (VUNS) in the Operation mode.

The following calculations are made in the Operation mode

$$W_S = W\cos(K + УС - УК - ЗПУ_i); \tag{11.13}$$

$$W_z = W\sin(K + УС - УК - ЗПУ_i); \tag{11.14}$$

$$U_y = W\cos(K + УС - УК) - U\cos(K - УК); \tag{11.15}$$

$$U_x = W\sin(K + УС - УК) - U\sin(K - УК); \tag{11.16}$$

$$U = \sqrt{U_x^2 + U_y^2}; \tag{11.17}$$

$$\delta = \arcsin\frac{U_x}{U}; \tag{11.18}$$

$$z_i = \int_0^t W_S dt; \qquad (11.19)$$

$$S_i = S_{ni} - \int_0^t W_S dt. \qquad (11.20)$$

the values of U, δ, U_x and U_y should be calculated so that these variables can be stored and used upon transition in the Memory mode.

The values of W and US are not measured in the Memory mode. Therefore, the values of wind parameters and the air speed sensor signal U stored in the Operation mode are used. The following formulas are used:

$$W_S = [U\cos(K - УК) - U\cos\delta]\cos ЗПУ_i + [U\sin(K - УК) + U\sin\delta]\sin ЗПУ_i; \qquad (11.21)$$

$$W_z = [U\cos(K - УК) + U_y]\sin ЗПУ_i - [U\sin(K - УК) + U_x]\cos ЗПУ_i. \qquad (11.22)$$

The aircraft coordinates S-z are calculated as before by formulas (11.19) and (11.20).

The Turn mode begins when some distance to the next PPM (linear lead of turn--LUR) remains to the aircraft. The origin is converted in this mode. Recalculation is made by the formulas

$$S_{n(i+1)} = \sqrt{(x_{n(i+2)} - x_{n(i+1)})^2 + (y_{n(i+2)} - y_{n(i+1)})^2}; \qquad (11.23)$$

$$\sin ЗПУ_{i+1} = \frac{x_{n(i+2)} - x_{n(i+1)}}{S_{n(i+1)}}; \qquad (11.24)$$

$$\cos ЗПУ_{i+1} = \frac{y_{n(i+2)} - y_{n(i+1)}}{S_{n(i+1)}}; \qquad (11.25)$$

$$S_{i+1} = S_{n(i+1)} + S_i\cos(ЗПУ_i - ЗПУ_{(i+1)}) - z_i\sin(ЗПУ_i - ЗПУ_{i+1}); \qquad (11.26)$$

$$z_{i+1} = S_i\sin(ЗПУ_i - ЗПУ_{(i+1)}) - z_i\cos(ЗПУ_i - ЗПУ_{(i+1)}). \qquad (11.27)$$

Further, operation by formulas (11.13)-(11.20) continues in the new S-z coordinate system.

Precise values of S-z are calculated in the Correction mode by the formulas:

$$S_i = D\cos(A - ЗПУ_i - \Delta N_i) - S_{\text{м}i}; \tag{11.28}$$

$$z_i = D\sin(A - ЗПУ_i - \Delta N_i) - z_{\text{м}i}, \tag{11.29}$$

where all notations were determined previously and

$$S_{\text{м}i} = (x_{\text{м}i} - x_{\text{п}(i+1)})\sin ЗПУ_i + (y_{\text{м}i} - y_{\text{п}(i+1)})\cos ЗПУ_i; \tag{11.30}$$

$$z_{\text{м}i} = (x_{\text{м}i} - x_{\text{п}(i+1)})\cos ЗПУ_i + (y_{\text{м}i} - y_{\text{п}(i+1)})\sin ЗПУ_i. \tag{11.31}$$

Thus, all integration errors by formulas (11.19) and (11.20) are eliminated after the correction is made.

The following variables should be formed in the Shortest distance mode of the VUNS:

$$D_i = \sqrt{s_i^2 + z_i^2}; \tag{11.32}$$

$$\sin ФПУ_i = \frac{z_i}{D_i}; \tag{11.33}$$

$$\cos ФПУ_i = \frac{S_i}{D_i}. \tag{11.34}$$

The coordinates of the next PPM are entered manually by the navigator rather than by the program method in the Manual input mode.

The :ulations required for navigation are organized in the form of an iteration proc..s and the number of the next PPM serves as the iteration indicator. It was feasible in the example under consideration to organize yet another step of the iteration process for alternate calculations by formulas (11.7)-(11.34). This permits a sharp reduction in the number of resolving components in the VUNS. The uniqueness of most of the given formulas (the Pythagorean equations or coordinate conversion formulas) indicates the effectiveness of this solution.

We proceed from the general structure presented in Chapter 8 in synthesis of the VUNS. We organize the necessary calculations in the RCh [Resolving part]. We provide organization of the IT [Iterative process] by using the UZ. This distribution of functions is standard. Let us proceed from the product of the IM [Iteration machine] being designed in synthesis of the RCh.

The values of U, δ, sin ZPU$_i$, sin FPU$_i$, cos ZPU$_i$ and cos FPU$_i$ will be found as a result of a multistep calculating process at the output of special operational analog memory cells and will be transmitted to the nonvolatile ZU [Memory] (DZU). Four ZYa [Memory cell] are required in the DZU since the same cells can be used for the ZPU and FPU as a function of the operating mode. These can be ordinary ZYa (§ 5.7) without regeneration with regard to the real speed of the RE. Since can assume any value in the range of 0-360°, a double ZYa can be used for δ: $\delta - E(4\delta/\pi)$ should be stored in the ordinary ZYa and $E(4\delta/\pi)$ should be stored in the special ZYa, where $E(4\delta/\pi)$ denotes the entire part of the number in parentheses. The multistable element of § 5.8, for example, can be used as this cell.

Let us form variables S_i and z_i in integrator-interpolator types cells (see § 1.6 and 8.2). Since variables S_i and z_i are used directly for navigation, high resolution is required. This is accomplished by using double ZYa, which are a combination of an ordinary integrator with dump and multidigit counter. A diagram of this cell is given in Figure 11.14.

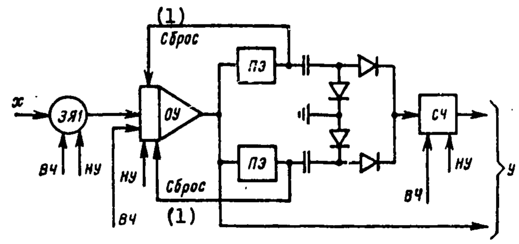

Figure 11.14. Integrator-Intepolator Cell With Combined Display of Output Value: ZYa1--input ZYa for storage of derivative; VCh--input number bus; NU--number input resolution bus; OU--high-quality operating amplifier-integrator; PE--high-quality comparators for display and positive and negative overflow; SCh--unitary reversible pulse counter (§ 6.1); x--input variable; y--output variable

Key:
1. Dump

A subintegral function which is retransmitted to the ZYa1 is formed periodically in the special operating memory cell when the circuit is operating. Integrator OU then performs integration. Overflow OU is initiated by one of the PE. This PE dumps U to the zero position and simultaneously transmits a pulse to the reversible counter. The given ZYa circuit for S and z provides good resolution. But the accuracy of calculations is determined by the accuracy of the OU. If accuracy must be increased, the deviation W_s from the mean value $\bar{W}_s$ rather than W_s must be integrated.

Thus, the total product of the VUNS is formed in the DZU, including six ZYa. Three of them are ordinary and are used to store V, sin ZPU (or sin FPU) and cos ZPU (or cos FPU). One is combined for storage of $\dot{S}$ and two are integrators-interpolators with combined display of variables. It should be pointed out that the composition of the DZU is clearly determined by the selected common structure and designation of the IM. Informal decisions were made only on problems of providing accuracy and resolution. The basis for these decisions were the concepts outlined in Part 2.

By introducing unitary variable m_1 by the ordinary method, which controls operation of the DZU, we provide the relationship of the states of the DZU and this variable indicated in Table 11.9. Organization of this DZU with regard to the contents of Part 2 is trivial. Since no more than six numbers are entered simultaneously in the DZU (six numbers are entered at $m_1 = 10$), it has a total of six input buses. Distribution of the input buses by cells is natural.

Table 11.9.

№ m_1	Функция ДЗЯ (1)					
	S	z	U	sin ηy	cos ηy	δ
1	(2) И	И				
2	31	И				
3	И	31				
4	И	И	3			
5	И	И		3		
6	И	И			3	
7	И	И				3
8	И	И				
9	33	33				
10	33	33				

Key:
1. Function of DZYa
2. Integration

Note. I--integration; Zl--input of number into ZYal; 33--input of numbers into ZYal, OU and SU (see Figure 11.14); 3--input of number; empty space--storage

In the given case the OZU includes six standard analog ZYa. It is controlled by means of unitary instruction m_2, which assumes seven different values. The number is entered in the cell having the corresponding number at m_2 = 1-6. All cells store the stored numbers at m_2 = 7.

Other versions are also possible with selection of the number of OZU cells. If one rejects simultaneous entry of the initial values of S and z, one may have only three ZYa in the OZU. An additional instruction m_1 is required in this case and the tracking function is complicated somewhat. Taking these concepts and the relative simplicity of the OZU into account, a version with six cells was adopted. It was pointed out in § 5.7 that the ZYa can perform upon entry of the number different operations with the entered number and contents. However, a single operation--entry of the number--has been adopted for the OZU. This solution was adopted on the basis of selection of variants.

The operations indicated in formulas (11.7)-(11.20) must be fulfilled to fill the OZU cells, for example, it is sufficient to calculate the subintegral expressions for (11.19) and (11.20). These calculations are made by a special RE which has been called the operating block (OB). During selection of the variants, one was initially oriented toward the OZU with total set of operations. The following variants of the OB were considered:

1) with minimum number of RE (sin, multiplier and two operating amplifiers). This variant generates complex programs, complicates the OZU and does not provide the necessary speed;

2) with number of RE which provides solution of any equation during one step (2sin, seven multipliers and four OU). This version is intriguing, but does not provide the necessary dimensions;

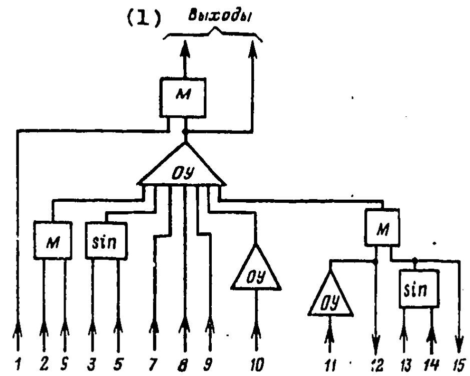

Figure 11.15. Diagram of Third Variant of Operating Block of Aircraft Navigation Computer: M--multiplier; sin--functional converter of type; OU--operating amplifier

3) with number of RE selected so as to provide calculation of any function of (11.10)-(11.20) in no more than three steps. This version was the most acceptable. A diagram of the OB of this version is given in Figure 11.15.

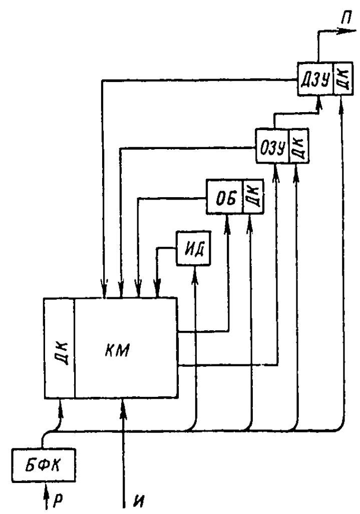

Figure 11.16. Block Diagram of Aircraft Navigation Computer: BFK--instruction formation block; DK--instruction decoder; KM--switching matrix; ID--data storage and input device; OB--operating block; OZU--internal storage; DZU--non-volatile memory; R--data on flight mode; I--measurements; P--product

The mathematical functions are formed by organization of the necessary connections of the OB inputs to the OZU, DZU and OB outputs and the output of the input data block. Further synthesis consisted in formal compilation of a list of the states of the switching matrices, writing the tracking tables and making more specific the volume of the universal structure with respect to the given problem. Despite some cumbersomeness of this process, it was completed within several days by a single executor. As a result a VUNS was synthesized, the approximate weight of which in the microelectronics version comprises 1 kg and a volume of 300 cm^3. A block diagram of the VUNS is given in Figure 11.16. Compared to the general structure given in Chapter 8, it contains the following main simplifications:

1) nonadjustable instruction decoders DK are used in place of the PDK;

2) the BFK locking device has no cognitive completion functions. A fixed sequence of control signals coming directly to the DK is formed in it;

3) the ID block (the PTK of the common structure) and the DZU and all the DK have no relationship to the KM lines.

[108-6521]

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PROBLEMS OF HYBRID COMPUTER TECHNOLOGY

Kiev PROBLEMY GIBRIDNOY VYCHISLITEL'NOY TEKHNIKI in Russian 1979 signed to press 20 Dec 79 pp 2, 167-168

[Annotation and table of contents from collection of scientific works, Izdatel'stvo "Naukova Dumka," 290 copies, 168 pages]

[Text] In this collection are discussed questions relating to the development of computing and peripheral hardware of hybrid systems. The results are given of an investigation of parallel digit-oriented structures for solving linear equations. Also discussed are questions relating to the reliability and testing of computing system units and modules.

Intended for scientific and engineering and technical personnel specializing in the area of developing hybrid computer technology hardware.

CONTENTS

[82-8831]

8831
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SOFTWARE

AUTOMATED PRODUCTION OF APPLIED PROGRAM PACKAGES

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 203-207

[Table of contents from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

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[110-6521]

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APL/M FOR ELEKTRONIKA-60

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 5-8

[Article by S. P. Prokhorov from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

[Text] Reference is usually made to clever methods of formal description of the syntax and semantics of programming languages in papers devoted to translator design systems. These methods, effective and useful in realization of translators with high-level languages, become extremely cumbersome, however, if one is talking about realization of languages having no formal description (FORTRAN) and also instrument and machine-dependent languages. To realize them, it is desirable primarily to have a copious bibliography of systems programs and an access language to it in the computer which permits rather simple and convenient description of the semantics of individual structures of the language.

Problems of the portability of software are also related directly to this. There is a number of papers devoted to the problem of what a language should be, which on the one hand is convenient for writing translators and on the other hand is sufficiently simple for realization on a specific computer. The method now proposed by a number of foreign authors for using p-codes, which are essentially some fixed set of procedures used by systems programmers, supplemented by the mnemonics of access to them, is a successful practical approach which permits development of mobile computer systems. However, even in this case it is first necessary to realize a sufficiently large number of procedures on the computer.

The use of interactive systems realized on the basis of high-level languages (SETL and APL) permits significant acceleration of the work to develop specialized languages and also the software for new machines due to the fact that they (SETL and APL) are highly expressive and moreover one can avoid consideration of problems related to lexical and syntactical analysis of programs, editing and file management during development of the systems. The dialogue mode in combination with the developed debugging facilities permits one to rapidly produce a high-quality product.

The specifics of the new machines is the absence of simple and convenient debugging facilities on them and also intelligibly described documentation. The use of APL permits one to obtain an objective code, thus avoiding the difficulties with development of an assembler editor. Programming the program in APL for the processor

P consists in calculation of some file A, the value of which should be subsequently removed to some external carrier. For example, if we want to generate a code which will be obtained upon translation of the instructions of the PDP-11 assembler

MOV R1, R2

where R1 and R2 are the numbers of the registers, then all that we have to do is to write a similar function in APL

```
 ∇  MOV R
[1] A [COUNT] ←R[2] + 64 x R[1] + 64
[2] COUNT ← COUNT + 1
 ∇
```

As a result of fulfilling this instruction of the function in file A, the code of instruction to transfer the contents of the first argument to the second will be written. Let us note again that lexical and syntactical analysis (checking the correctness of access to the APL function MOV!) will be carried out by the APL system. The second no less important thing is that this "macrogenerator" written in APL permits more flexible access formats than any of the existing macroassemblers. For example, when writing the program one can use an explicit form of the files and complex expressions

MOV R1, V[COR + 1] + (V1[COR1] ÷ 2) x K

It is also easy to determine the program for arbitrary generation

```
∇MOV R
[1] →REG x 2P[j] < 10
[2] A [COUNT] ← P[2] + 64 x 23 + 64
[3] COUNT ← COUNT + 2
[4]  → 0
[5] PEG: A[COUNT] ← P[2] + 64 x P[1] + 64
[6] COUNT ← COUNT + 1
 ∇
```

If the first argument is less than 10 (register), then code generation is similar to the previous example, otherwise the instruction occupies two machine words.

Thus, description of the assembler is a problem requiring several days (if not hours) of work. No knowledge of APL whatever is required of the user working with the PAL generator.

Another approach includes realization of functions on the APL which, besides generation of the machine code (or instead of it), at the same time issue a program (or instead of it) in the APL-simulating work of the computer. The means of expression of the PAL are so vast that realization of p-codes (for example, p-codes developed at the University of Helsinki) is very simple. Usually one line of the APL is sufficient (and frequently even the use of a single function of the language is sufficient). Thus, high-quality debugging of the software can be accomplished even before the computer is obtained, while the interactive mode of operation permits this to be done simply and easily.

The technique outlined by the author for development of software is used to realize the APL/M programming system, which has been suggested for setup on the SM-4 and Elektronika-60. The APL/BESM system was supplemented especially for this purpose for systems problems by introducing the systems concepts of structure and type and some set of baseline functions was determined which are adequate to describe the set of all the structural transformations permissible in the APL. The APL functions are rewritten in this "baseline APL." The use of this limited subset permits one to obtain "rigid" codes (since the type and size of the files are fixed). The algorithm is smoothed out. An objective code which will also be transferred to a minicomputer will again be obtained for the resulting program by using the APL/BESM.

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DESIGN OF SYNTACTICALLY CONTROLLED TRANSLATORS IN DIALOGUE TRANSLATOR DESIGN SYSTEM--EL'BRUS APPLICATION

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 8-12

[Article by S. M. Abramovich and Kh. D. Dzhenibalayev from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

[Text] 1. Considerable progress has been achieved in production of translators with algorithmic programming languages: there are formal models, different algorithms for realization of language structures, program blanks and finally SPT [Translator design system] [1, 2] which fix separate regulations and which automate various aspects of translator development. Despite all this experience and the rather abundant arsenal of facilities, development of a translator is still a laborious and prolonged process which requires many man-years.

One of the reasons for this situation is that formal models are rather abstract and the algorithms, program blanks, methods and so on usually describe some idealized medium of using them. When developing a specific translator, all this should be modified and adapted to specific conditions (the language, machine, operating system, standards adopted in the SPT and so on). The experience accumulated during development of specific translators can be used to the maximum degree--up to borrowing the data structures, syntax fragments, transducers (semantic programs) and so on--is feasible.

The second reason which makes it difficult to use the accumulated experience is that the process of developing a translator is largely routine in nature and consists of a mass of nonessential "details" of a technical nature, an enormous number of which is frequently transformed to a problem. The need to automate this aspect of translator development is obvious.

Yet another of the no less important factors which make it difficult to use available experience is the difficulty of operational access to the information required at a given moment, even if it is represented in well-structured documentation. Automation of access to the required data can provide sufficiently rapid, selective formation of the required information in the most complete volume and suitable form. This process is preferably carried out in the dialogue mode as the most operational and natural for the human method of communication.

2. An approach to the configuration and technique of using SPT which permits to some extent solution of the problems postulated above is proposed in the given article.

The initial prerequisites of the proposed approach to development of SPT are the following: the existence of some set of established designs which are present in one or another form in most available and newly developed programming languages, the existence of accepted methods of realizing these designs (identification with block structure in the languages, realization of recursive procedures, priority analysis and so on), the existence of accepted schemes for organization of syntactically controlled translation (used in development of production translators), based on sequential irreversible review of the text to be translated.

The proposed SPT is designed for use for the following purposes: teaching methods of realizing typical constructings of common programming languages, development of a translator for a high-level programming language created within this SPT or given externally, the author's accompaniment of the developed translator and modification of the developed translator both by the authors and by a special group of accompaniment.

3. Let us consider in general terms the technique of using the proposed SPT to develop a translator from some high-level language.

The step of developing the basis of the translator. In the dialogue mode which the SPT conducts, the user selects from the language constructions of the reference language of the SPT available in the SPT archive those whose semantics coincides or is similar to the semantics of some language constructions, thus developing the language base. The constructions are recalculated by the SPT in terms of established concepts of common programming languages (expression, cycle operator, conditional operator, operation priorities and so on) with indication of the section to which it is related (data, operations, operators and so on). Based on the constructions selected by the user, the SPT separates the translator base from the reference translator of the SPT and the language base from the reference language. This step can be final if the language base coincides with the language and if the user has no need to change its vocabulary, syntax and realization.

The step of studying realization of the language base in the translator base. In the dialogue mode the SPT determines (in some fixed order or the order determined by the user) the construction from the language base and issues the vertical layer corresponding to realization of it [3]. The vertical layer is the aggregate of texts in the syntactical control metalanguage (MSU) and in the instrument language (Ya). The MSU is designed to record the syntax with indicators to the transducers which accomplish cognitive processing of the text. The text in the instrument language is the transducer text, the text of data descriptions with which these transducers operate and so on.

The step of language base and translator base changes. The user indicates the construction of the language subject to change. He then rewrites fragments of the layer requiring changes and also the corresonding fragments for describing the language base and the SPT and enters these changes in the translator base and language description. Thus, the semantics, syntax and vocabulary of the language base constructions and realization of them can be changed.

The step of additions to the language base and translator base. The user describes the newly developed constructions with indication of the section to which this construction is related and the SPT enters the corresponding changes in the description of the language base. It then writes the vertical layer which realizes the added construction and the SPT enters the fragments of this layer in the appropriate positions of the texts in the MSU and instrument language.

We note that the translators mentioned above are actually flow charts, i.e., they are the texts in MSU and instrument languages. The SPT can translate from these languages at any of the enumerated steps, upon instruction of the user, and can assemble a translator in objective code from the flow sheet. At the same time, a modified version of the SPT is also developed in which the role of the reference language and the reference translator are played by the language and translator bases, respectively. Because of this, all capabilities offered by the reference SPT can be used at the steps of study and accompaniment of the developed translator.

A nonprofessional user (not familiar with MSU and instrument languages) can also use the proposed SPT to develop translators from simple specialized programming languages. Naturally in this case the changes and additions which can be entered in the language base created after the first step are sharply limited. Thus, for example, he can change the external display of service words and the priorities of operations and can add new operations by indicating the sequence of instructions of the object machine described in the form of macrodefinitions, which realizes them.

4. From the viewpoint of configuration, the proposed SPT consists of the following components: MSU-translator designed to translate the MSU-text to the syntactical control table, on the basis of interpretation of which syntactical control is accomplished in the translator being developed, the instrument language-translator from instrument language, the flow sheets of the reference translator from the reference language, which is a set of unified language constructions which cover the constructions of a number of known programming languages, the aggregate of relationships which link description of each language construction of the reference language to the fragments of the reference translator which realize it and the monitor, under the control of which the user communicates with the SPT in the dialogue mode.

A preliminary design of the described SPT for the El'brus MVK is now being developed. A modification of the MSU-language of the RGU SPT is used as the MSU-language in it [2] and the El'brus MVK autocode is used as the instrument language [4].

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TRANSLATOR FROM EL'BRUS-1 MVK AUTOCODE--MODEL AND REALIZATION

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 76-78

[Article by I. F. Lesovaya, V. N. Polivanov, N. A. Shishova, V. V. Okol'nishnikov, V. A. Mozzherin and V. A. Markov from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

[Text] The purpose of the report is to show the main elements of the technique used in development of the production translator from the El'brus-1 multiprocessor computer complex (MVK) autocode.

The El'brus-1 MVK autocode. This is a machine-oriented high-level language. It is far superior to ALGOL-60 in nomenclature of the basic values which control and process the constructions and is similar to ALGOL-68. For example, it contains values of the procedure type.

The El'brus-1 MVK. This is the first domestic fourth-generation computer in the large machine class. The main configuration features are multiprocessor capability (universal and specialized processors), apparatus stack, context security of data and tagged memory.

Technology. The evolution of development of traditional methods is analyzed in the report after the characteristics of the language and the machine. It is pointed out that a specific transformation of goals (the software crisis and the concept of a programmed product) occurred in the field of construction of production translators as well as of software as a whole. It is concluded that traditional methods largely waste their adequacy in the context of new goals to construct translators from new-generation languages (post-ALGOL extensive languages of the El'brus-1 MVK autocode or ALGOL-68 type).

The authors feel that the proper activity of the translator developer under the new conditions, which provides success not only of production but of accompaniment as well, should be reproductive. This requires conceptualization of the translator and the technique which supports this conceptualization.

Two parts--conception and organization of work--are determined in the technique used by the authors.

The main essence of both parts of the technique are advanced sequentially in the report. The systems concept of the translation process and a model of the translator which supports this concept are formulated in the first part.

The systems concept is "soft execution of the entry line." Soft execution is one of the possible specific aspects of the fundamental principle of mixed calculations.

The translator model is the so-called recursive programmed machine. Its main components are the control device, called the control machine in the model, a set of actuating members organized by the principle of desk calculators, the local control device which links the actuating members to each other and to the control device and the last component is the memory.

Organization of operations is subordinate to the concept and is completely presented in the report.

The report ends with the section on realization. Problems of the adequacy of display of the constructed model in the set of concepts of the realization language are discussed. The degree of adequacy achieved in display of the translator model from the El'brus-1 MVK autocode to devices accessible in the YaRM02.5 preprocessor and in YaRM02 high-level machine-oriented language, is evaluated. The control machine and the vocabulary calculator are displayed in the YaRM02.5 in this case, while the operating and pragmatic calculators are displayed in the YaRM02.

An example of the complete functioning of the translator is given in the conclusion.

The translator from El'brus-1 MVK autocode operates within the framework of the TEMP instrument complex, which simulates the capabilities of the El'brus-1 MVK on the BESM-6 computer, and which has been in operation since early 1979.

The time of developing the translator comprises approximately two years, the dimensions are on the order of 50,000 lines in the YaRM02 and productivity is 1,000-1,500 lines/min. The translator was used to develop translators from ALGOL-60 and standard FORTRAN, which were then converted and began to operate in real El'brus-1 MVK.

A translator consisting of the TEMP instrument complex has now been introduced and is being used in many organizations of Moscow, Leningrad, Rostov-na-Donu and so on.

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REALIZATION OF THE FIRST VERSION OF THE CROSS SPT ON THE BESM-6 COMPUTER

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 180-182

[Article by V. I. Gololobov and V. A. Isayev from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

[Text] The first version of the CROSS SPT is described in the report. The first version of the CROSS SPT is oriented mainly toward writing single-pass translators from languages, the external (user) descriptions of which are made by means of expanded BNF-notation. The CROSS SPT includes an input language, preprocessor from the input language to the base language and procedural materials containing descriptions of the methods of diagnosis and restoration of the analysis process in detection of syntactical errors by means of the input language.

The input language of the CROSS SPT offers means to describe the language being realized which are adequate to external descriptions, means of describing the vocabulary in a form close to the assignment of regular expressions, means of describing syntax by using the expanded BNF-notation and means of assigning semantic actions for syntactical constructions.

The input language of the CROSS SPT is the superstructure over the base language which provides means of describing the translation process.

High-level machine-oriented language (on the BESM-6) YaRMO was used as the base language in the present realization. The YaRMO offers means of program segmentation, assignments of the mechanism of procedure calls and modular organization of the program.

The translator from the input language of the CROSS SPT is realized as a preprocessor which translates the input program to YaRMO language. The preprocessor, processing the input program, gathers the required information into tables, forms the corresponding YaRMO fragments, adds the standard module--syntactical and vocabulary analyzers--to them, thus forming the program in YaRMO language.

The program is found in machine code as a result of operation of the YaRMO translator, which specifically contains the following sections:

--the syntax program written in universal form by means of so-called syntactical instructions, which in compressed form is the syntax of the input language and indicates the semantic subprograms related to the syntactical constructions,

--the vocabulary-ordered list of all terminal displays of language (for example, "beinning," ":=." "+" and "=,"

--the diagram of states which describes the vocabulary of the input language whose structure is similar to that described in [1].

The syntax analyzer, interpreting the syntax instructions, selects the input line and starts the required semantic subprograms. The vocabulary analyzer is accomplished by the diagram of states. The longest terminal display is first read from the input flow by means of a list of terminal displays (for example, if there are terminal displays ":=" and ":" in the language, then ":=" will be read from the input flow ...:=1;... . If an arc tagged by the read terminal display is not determined from the initial state to the diagram of states, vocabulary analysis is assumed to be completed. Otherwise (for more complex vocabularies), the analysis is continued by the diagram of states.

This scheme of analysis requires a large amount of work related to searching in various tables and practically any search in the translator reduces to determining the entry of the terminal to some set.

The affiliation matrix, to each terminal in which a line corresponds, and to the set of which a column corresponds, is created for the maximum acceleration of these searches. The matrix element gives the feature of entering the terminal in the set. Introduction of the affiliation matrix completely solved the problem of search and fast switches during analysis.

Each line of the affiliation matrix occupies two cells of the BESM-6 in the translator from El'brus autocode in the TEMP instrument complex written by using the CROSS SPT. The expenditures of memory on the affiliation matrix are totally compensated for by economical internal display of the syntactical and vocabulary structure of the language. The size of translators written using the CROSS SPT does not exceed the size of translators realized by other methods.

An interpretation scheme for analysis which provides great flexibility and reliability when using the affiliation matrix has sufficiently high-speed characteristics. Thus, the translator from El'brus autocode to TEMP IK [Instrument complex] operates at a speed of 1,000-1,500 lines per minute.

Printing the track of syntax and vocabulary analysis and gathering of statistics on the frequency of performing the constructions, which permit the developer to optimize the translator more efficiently, play the main role among the debugging equipment.

The system is now in operation and further investigations are being carried out to improve and develop the system and realization of versions of the SPT for other base languages and machines.

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THE MIS SYSTEM--EL'BRUS APPLICATION

Tallinn AVTOMATIZATSIYA PROIZVODSTVA PAKETOV PRIKLADNYKH PROGRAMM in Russian 1980 (signed to press 24 Jul 80) pp 187-188

[Article by A. Lomp, M. Kharf and A. Shmundak from collection "Automated Production of Applied Program Packages", edited by A. Vooglayd, Tallinskiy politekhnicheskiy institut, 600 copies, 208 pages]

[Text] Development of a mobile programming system (mobile interactive synthesizer --MIS) is described, the prototype of which is the PRIZ YeS programming system.

PRIZ type systems are designed to describe the semantic relationships between objects and to synthesize programs from these descriptions. They are well adapted for use as means of interaction between the user and applied program packs. The MIS system is being developed to work in the El'brus MVK [Multiprocessor computer complex]. However, it was noted during development that modern PPP [Applied program pack] for solution of scientific and technical and engineering problems are usually realized in FORTRAN and consequently are rather easily transferred from one type of computer to another. In view of this, it was decided to develop a mobile system. FORTRAN GOST, the translator from which is contained in the first unit of the El'brus MVK MO and the interfaces with the operating systems (mainly input-output) are localized in a small number of modules, was selected as the realization language. This organization made it possible to organize the system for the YeS EVM [Unified computer system].

Dialogue programming systems are now acquiring ever greater popularity. The MIS system was designed so that it can operate both in the pack mode and in the dialogue mode. As in previous versions, the user has access to archives for storage of the descriptions of his own computer models in a form which permits, on the one hand, rapid starting of the program, and on the other hand, restoration of the text of the model description. A context editor which permits operational correction of both the current model and the contents of the archive, is offered for working in the dialogue mode.

The UTOPIST language used by the system was also changed. Determination of the method of realizing the relationship should primarily be noted. Moreover, the capabilities of program synthesis have been expanded by addition of synthesis of simple cycles.

The problem of realization of the macroprocessor to UTOPIST language is considered.

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FUNDAMENTALS OF THE OPERATING SYSTEM OF THE UNIFIED COMPUTER SYSTEM

Moscow OSNOVY OPERATSIONNOY SISTEMY YES EVM in Russian 1980 (signed to press 11 Aug 80) pp 2-3, 144

[Annotation, foreword, bibliography and table of contents from book "Fundamentals of the Operating System of the Unified Computer system", by Adol'f Aleksandrovich Zemlyanskiy and Mikhail Grigor'yevich Persits, Izdatel'stvo "Sovetskoye radio", 40,000 copies, 144 pages]

[Text] Applied problems of using the operating system of the YeS EVM [Unified computer system] are outlined in the book. The general functions and composition of the OS YeS [Operating system of the unified computer system] are considered and the assignment control language and systems processing programs are described. Examples are presented which illustrate the material and can be used by programmers for solving practical problems in the operating system of the unified computer series. The book is intended for programmers familiar with one of the programming languages of the operating system. It can be recommended to personnel desiring to master independently the procedures for working with the OS YeS and also to students of vuzes of the corresponding specialties.

Foreword

Modern computers are equipped with a set of programs which facilitate the problem preparation process and which provide running of problems through the machine. The software of modern computers makes it possible to coordinate the work efficiently, to distribute resources optimally, to provide information input and output, to debug programs and to detect and diagnose errors.

The unified series (YeS) of computers has developed software at its disposal, among which the central position belongs to the operating system (OS).

The authors did not attempt to provide detailed description of the capabilities of the operating system of the YeS EVM, but attempted to outline the necessary minimum of data that can be used to begin practical utilization of it.

The first chapter of the book is devoted to the main concepts of the OS of the YeS EVM. It contains brief information on the composition and functions of the system, the control program and assignment control and problems of organization of data and control of them are also considered.

The material of the second chapter is devoted to the assignment control language--a powerful and effective means of planning and control of computer operation. This part of the book functionally fulfills a double load: on the one hand, it can be used for practical work and on the other hand it serves as reference material. The rules for encoding of control operators are described and the control operators themselves are considered in the chapter.

Information on systems processing programs is outlined in Chapter 3. The main steps of programs in the operating system--translation, editing of communications and debugging--are considered here. A considerable position is given to the step of program translation from different languages included in the OS YeS EVM.

The book contains many examples which encompass the situation most frequently encountered in practice.

Exhaustive material on the operating system can be found in the operational documentation of the OS YeS, while the required operating languages of the system are acquired during practical work on the machine.

The authors feel it their pleasant duty to express gratitude to Professor V. N. Chetverikov and to candidates of technical sciences Yu. S. Belyavskiy, A. A. Ivanov and G. N. Revunkov for review work and for valuable comments on the manuscript.

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BASIC SOFTWARE OF AN AIR-SPACE DATA PROCESSING COMPLEX

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 61-66

[Article by N. S. Yakovenko, Novosibirsk]

[Excerpts] Introduction. The basic computer of a complex for processing astro- and aerophotographic surveys (information about the hardware of the complex is contained in [1] and its bibliography), realized on the basis of the "Zenit-2," is the YeS-1010 mini-computer, the functions of which include control of the complex through the CAMAC apparatus); primary processing of data obtained on the "Zenit-2" automatic machine; control of "operative visualization" of information (a CAMAC monitor and color and half-tone TV CAMAC displays are included in the complex); assuring the transmission of information (through a standardized main-line exchange system for subsequent processing (on the M-4030, NR2116V and M-6000 computers) or output to specialized peripherals (the "Planshet" plotter and the "Karat" microfilming device).

The present article has the purpose of describing program modules belonging to the lower level of software of the complex (basic modules) which are engaged in direct control of a functionally separated specific part of the automation. They are written in Assembler and can be summoned from modules of a higher level which accomplish preliminary data processing or combine the functioning of various parts of the complex and are recorded either also in Assembler or in the higher-level language PLR-10 or FORTRAN-IV.

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DEVELOPMENT OF AN AUTOMATED CONTROL SYSTEM FOR THE ECONOMY OF AN ADMINISTRATIVE REGION

Riga SOZDANIYE AVTOMATIZIROVANNOY SISTEMY UPRAVLENIYA EKONOMIKOY ADMINISTRATIVNOGO RAYONA in Russian 1980 (signed to press 17 Mar 80) pp 2, 150-151

[Annotation and table of contents from collection edited by A. Viyesis, Latviyskiy gosudarstvennyy universitet imeni P. Stuchki, 290 copies, 152 pages]

UDC 65.011.56:33(-2/-5)

[Text] The republic interagency collection of scientific works is devoted to study of the theoretical and practical problems of development of territorial ASU [Automated control systems]. The collection is published annually. The results of scientific research are presented by instructors of vuzes, postgraduate students, colleagues of leading scientific research institutes and specialists of computer centers. Problems of ASOD [Automated data processing system] design for an administrative rayon and ASGS [Automated system for state statistics] and ASPR [Automated control system for planning calculations (under Gosplan)] subsystems and also the capabilities and advantages of using the latest computer equipment, different data carriers, data transmission systems and economic methods of analysis are considered in most articles.

The collection of scientific articles can be recommended to instructors and students of vuzes, colleagues of computer centers and rayon administrative, planning and statistical bodies.

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CHARACTERISTICS OF THE MAIN COMPLEXES OF PROBLEMS OF THE FIRST UNIT OF THE ASOD OF VALMIYERSKIY RAYON

Riga SOZDANIYE AVTOMATIZIROVANNOY SISTEMY UPRAVLENIYA EKONOMIKOY ADMINISTRATIVNOGO RAYONA in Russian 1980 (signed to press 17 Mar 80) p 3

[Article by E. Ya. Vanags, Latvian Branch of Scientific Research Institute of USSR Central Statistical Administration, Riga, from collection edited by A. Viyesis, Latviyskiy gosudarstvennyy universitet imeni P. Stuchki, 290 copies, 152 pages]

[Excerpt] In December 1978 an interagency committee accepted for industrial operation the first unit of the automated data processing system (ASOD), Valmiyerskiy Rayon, containing four subsystems:

--ASOD for local bodies of state statistics;

--ASU [Automated control system] for rayon agriculture;

--ASU for the rayon association Goskomsel'khoztekhnika [State Committee of Agricultural Equipment and Machinery], Latvian SSR:

--ASU of raypotrebsoyuz [Rayon union of consumers' societies].

The composition of the first unit of the ASOD of Valmiyerskiy Rayon was determined by the complex program for development of the Latvian RASU [Republic automated control system], based on the feasibility of development of ASU, the volumes of economic data at enterprises and organizations and also the presence of the required resources for development of an automated system.

The total composition of the first unit of the ASOD of Valmiyerskiy Rayon includes 22 complexes of problems, of which 11 are related to bookkeeping and accounting, 3 are related to statistical accounting, 5 are related to planning, 2 are related to forecasting and 1 is related to pedigree record-keeping. Third-generation and also second-generation computers, keypunch machines and keyboard calculators are used to solve the complexes of problems of the first unit.

[104-6521]

6521
CSO: 1863

CALCULATING THE ECONOMIC EFFECTIVENESS OF THE AUTOMATED DATA PROCESSING SYSTEM FOR VALMIYERSKIY RAYON

Riga SOZDANIYE AVTOMATIZIROVANNOY SISTEMY UPRAVLENIYA EKONOMIKOY ADMINISTRATIVNOGO RAYONA in Russian 1980 (signed to press 17 Mar 80) pp 22-31

[Article by I. Ya. Vanags, Latvian Branch of Scientific Research Institute of USSR Central Statistical Administration, Riga, from collection edited by A. Viyesis, Latviyskiy gosudarstvennyy universitet imeni P. Stuchki, 290 copies, 152 pages]

[Text] The economic effectiveness of the ASOD [Automated data processing system] of Valmiyerskiy Rayon was calculated according to a method developed at the Latvian Branch of NII TsSU SSSR [Scientific Research Institute of Central Statistical Administration of the USSR].

The sources for obtaining the input data required to calculate the effectiveness were planning documentation, planning and fiscal report data of the Valmiyerskiy RIVTs [Rayon Information-Computer Center], statistical reports of enterprises and organizations of Valmiyerskiy Rayon, data of special investigations, norms and standards, current price lists and indicators of analogs.

The method of data processing at the rayon information-computer station with punch-card machinery as the main equipment was taken as the basis for comparison. The different types of expenditures for data processing were taken into account into the variants being compared.

The capital investments for development of the ASOD for an administrative rayon consist of the cost of RIVTs equipment, expenditures for construction of the RIVTs building and preproduction expenditures.

The cost of equipment (K_{ob}), based on the composition and amount of computer and other equipment, the cost of a unit of equipment and transport and installation expenses, was determined at 2,015,800 rubles.

Expenditures for construction of the RIVTs building (K_{zd}), according to the contract-detail design for construction of the building of the Valmiyerskiy RIVTs, comprise 784,000 rubles and the preproduction expenditures (K_{pr}) were determined at 1,070,000 rubles.

The total capital investments for development of the ASOD (K_{or}) are calculated by the formula:

$$K_{sr} = K_{ob} + K_{zd} + K_{pr} = 2{,}015{,}800 + 784{,}000 + 1{,}070{,}000 = 3{,}869{,}800 \text{ rubles.}$$

The annual current expenditures for data processing in the ASOD for an administrative rayon includes the annual operating expenditures for data processing at the RIVTs, expenditures for solution of problems of the rayon automated system at the republic level and preproduction expenditures related to the annual period.

The operating expenses for data processing at the RIVTs consist of the personnel wages of the RIVTs, social insurance deductions, equipment depreciation deductions, expenditures for main and auxiliary materials, expenditures for spare parts and materials for routine and preventive maintenance of equipment, payments to the plant for computer repair, expenditures for electric power (for production needs), depreciation deductions for the RIVTs building and miscellaneous expenditures.

The personnel wages of the Valmiyerskiy RIVTs are determined on the basis of the makeup and number of workers, their official rates and tariff rates and the coefficient of the additional wage of operators (see Table 1). When establishing the official rates and tariff rates of workers, the circumstance that the Valmiyerskiy RIVTs has been converted to new wage conditions is taken into account.

The total wages for the year are 31,668 X 12 = 380,016 rubles.

Social insurance deductions (Z_s) for the workers in the TsSU system of the USSR comprise 5.5 percent of the wage fund:

$$Z_s = 380{,}200 \times 5.5 \text{ percent} = 20{,}900 \text{ rubles.}$$

The equipment depreciation deductions of the Valmiyerskiy RIVTs presented in Table 2 were calculated on the basis of the cost of the equipment and the corresponding norms of depreciation deductions.

Expenditure for main and auxiliary materials (M) are calculated at the rate of 2.0 percent of the cost of the main equipment (computers, hardware for data exchange and compilation and reproduction equipment):

$$M = 1{,}949{,}300 \times 2.0 \text{ percent} = 38{,}990 \text{ rubles.}$$

Expenditures for spare parts and materials for routine and preventive maintenance of equipment (V_t) are determined at the rate of 3.0 percent of the cost of the main equipment:

$$V_t = 1{,}949{,}300 \times 3.0 \text{ percent} = 58{,}480 \text{ rubles.}$$

Payment to the computer repair plant for preventive maintenance of punchcard machinery and keyboard computers of the RIVTs (according to the current price list for routine maintenance and preventive inspection of computers) comprises 16,100 rubles.

Consumption of electric power for production needs is calculated on the basis of consumed power and the annual fund of equipment operating time and comprises 462,920 kilowatt-hours.

Table 1. Calculation of Personnel Wages of Valmiyerskiy RIVTs

Name of Subdivision	Group of Workers	Number of Workers	Average Monthly Base Wage of Worker, rubles	Correcting Factor Which Takes Into Account Supplementary Wages	Total Monthly Wage, rubles (Group 3 X Group 4 X Group 5)
1	2	3	4	5	6
1. RIVTs manager	ITR (Engineering and Technical Personnel)	4	225	---	900
2. Miscellaneous administrative-management and service personnel	ITR (Scientific and technical personnel), salaried employees and MOP (junior service personnel)	18	110	---	1,980
3. Traffic control dept.	ITR	9	135	---	1,215
4. Algorithm compilation and programming dept.*					
a) planning group	ITR	3	140	---	420
b) programming group	ITR	5	150	---	750
5. Computer preventive maintenance dept.	ITR	30	145	---	4,350
6. Computer operation department	ITR	15	160	---	2,400
	operator	18	105	1.07	2,022

* When determining operating expenditures, only designers and programmers involved in working out designs and programs are taken into account. Expenditures for development of design documentation for new problems are included in capital investments for preproduction operations.

[Table continued on following page].

Table 1. (Continued from preceding page)

1	2	3	4	5	6
7. Department of automated data reception and transmission over communication channels	ITR	3	140	---	420
	operator	4	90	1.07	385
8. Central data preparation station	ITR	5	135	---	675
a) KVM (keyboard computer group	operator	39	85	1.07	3,547
b) group for preparation of machine data carriers	operator	59	90	1.07	5,682
9. Information receiving and production dept.	ITR	3	135	---	405
	operator	6	90	1.07	578
10. Copying and reproduction department	ITR	2	140	---	280
	operator	4	90	1.07	385
11. Normative-reference information dept.	ITR	3	140	---	420
	operator	3	90	1.07	289
12. Department for organization of processing accounting and statistics and statistical information production	ITR	6	140	---	840
	operator	3	90	1.07	289
13. Department for coordination of development and introduction of ASOC for administrative rayon	ITR	5	140	---	700
14. Peripheral data preparation terminals	ITR	6	135	---	810
	operator	20	90	1.07	1,926
Total		273	x	x	31,668

Table 2. Calculation of Equipment Depreciation Deductions of Valmiyerskiy RIVTs

Name of Equipment	Cost of Equipment, thousand rubles	Standard Depreciation Deductions, percent	Total Depreciation Deductions, thousand rubles (Col. 2 X Col. 3)/100
1. Main computer equipment	860,980	12,000	103,320
2. Additional computer devices	177,900	12,000	21,350
3. Equipment of central data preparation terminal	201,200	11,000	22,130
4. Equipment for peripheral data preparation terminal	71,080	11,000	7,820
5. Main hardware for data exchange	611,820	12,000	73,420
6. Miscellaneous hardware for data exchange	9,020	9,600	870
7. Reproduction and compilation equipment	17,270	8,100	1,400
8. Metal cutting and miscellaneous auxiliary equipment	10,000	9,900	990
9. Measuring and regulating devices and units	13,000	8,500	1,110
10. Autotransport equipment	11,000	21,900	2,410
11. Production and housekeeping inventory	32,500	12,500	4,060
Total			238,880

Expenditures on electric power for production needs at the RIVTs (V_e) with regard to the power utilization factor at the rate of 0.9 and the price of one kilowatt-hour of electric power at 0.025 rubles comprise:

$$V_e = 462{,}920 \times 0.9 \times 0.025 = 10{,}415 \text{ rubles.}$$

Since the standard depreciation deductions for the VTs building comprise 2.4 percent, the value of depreciation deductions for the building of the Valmiyerskiy RIVTs (A_{zd}) comprise:

$$A_{zd} = 784{,}000 \times 2.4 \text{ percent} = 18{,}820 \text{ rubles.}$$

Miscellaneous expenditures (P) are determined at the rate of 3.0 percent of the main (all previous) operating expenditures:

$$P = (380{,}020 + 20{,}900 + 238{,}880 + 38{,}990 + 58{,}480 + 16{,}100 + 10{,}420 + 18{,}820) \times 3.0 \text{ percent} = 782{,}610 \times 3.0 \text{ percent} = 23{,}480 \text{ rubles.}$$

Thus, the annual operating expenditures for data processing at the Valmiyerskiy RIVTs (S_e) comprise:

$$S_e = 782{,}610 + 23{,}480 = 806{,}100 \text{ rubles.}$$

The annual current expenditures for data processing in the ASOD for an administrative rayon (S_{sr}) are determined by the formula:

$$S_{sr} = S_e + S_r + \frac{K_{pr}}{T_g} = 806{,}100 + 25{,}000 + \frac{1{,}070{,}000}{12} = 920{,}300 \text{ rubles,}$$

where S_e is the annual operating expenditures for data processing at the RIVTs; S_r is the annual expenditures for problem solving of the ASOD at the republic level; K_{pr} is preproduction expenditures required for development of the ASOD; and T_g is the average period of use of preproduction expenditures in years.

Based on bookkeeping and accounting data of the Valmiyerskiy RIVS (and also of similar RIVS) with regard to the increase in the volume of information processed on punchcard machinery and keyboard computers and the increase of worker wages of the RIVS, the expenditures in the baseline version are determined at the following rate:

expenditures for equipment acquisition (K_o^b) are 680,000 rubles;

expenditures for construction of the RIVS building (K_{zd}^b) are 590,000 rubles;

preproduction expenditures (K_{pr}^b) are 340,000 rubles;

operating expenditures (S_e^b) are 775,000 rubles.

The capital investments required for data processing in the baseline version (K_b) comprise:

$$K_b = K^b_{ob} + K^b_{zd} + K^b_{pr} = 680,000 + 590,000 + 340,000 = 1,610,000 \text{ rubles.}$$

The annual current expenditures for data processing in the baseline version (S_b) are determined by a similar formula used in the version being compared:

$$S_b = S^b_e + \frac{K^b_{pr}}{T_g} = 775,000 + \frac{340,000}{12} = 803,300 \text{ rubles.}$$

An indirect saving--a saving in the production sphere at enterprises (organizations) of Valmiyerskiy Rayon, achieved with regard to the use of optimum, more complete, timely and reliable information--on the basis of expert estimates is determined at the rate of 1,140,000 rubles (0.5 percent of the cost of production, operations and services at enterprises and organizations of the rayon serviced by the RIVTs).

Additional investments required for development of the ASOD of Valmiyerskiy Rayon (K_d) are determined by the formula:

$$K_d = K_{sr} - K_b = 3,869,800 - 1,610,000 = 2,259,800 \text{ rubles,}$$

where K_{sr} is capital investments in the version being compared and K_b is capital investments in the baseline version.

The annual saving of current expenditures achieved as a result of functioning of the ASOD of Valmiyerskiy Rayon (E_t) is calculated as the sum of direct saving (E_p) and the indirect saving (E_k):

$$E_t = E_p + E_k - (S_b - S_{sr}) + E_k = (803,300 - 820,300) + 1,140,000 = = 1,023,000 \text{ rubles,}$$

where S_b is the annual current expenditures for data processing in the baseline version and S_{pr} is the annual current expenditures for data processing in the version being compared. The period of return of additional capital investments (T_{ok}) and the corresponding calculating factor of the economic effectiveness of additional capital investments (E_s) is determined in the following manner:

$$T_{ok} = \frac{K_d}{E_t} = \frac{2,259,800}{1,023,000} = 2.2 \text{ years;}$$

$$e_s = \frac{K_d}{E_t} = \frac{1,023,000}{2,259,800} = 0.45.$$

The annual saving achieved as a result of functioning of the ASOD of Valmiyerskiy Rayon (E) is determined by the formula:

$$E = E_t - K_d \times e_n = 1,023,000 - 2,259,800 \times 0.15 = 634,000 \text{ rubles,}$$

where e_n is the unified normative coefficient of the economic effectiveness of capital investments.

Calculation of the economic effectiveness shows the feasibility of developing the ASOD of Valmiyerskiy Rayon since the calculating factor of the economic effectiveness of additional capital investments for development of an automated rayon system is higher than the mean sector normative factor of the effectiveness of capital investments for development of the ASU and introduction of computer equipment established at the rate of 0.33.

[104-6521]

6521
CSO: 1863

APPLICATIONS

UDC 621.396.6.002.2:681.3

UTILIZING ELEKTRONIKA S5-12 MICROCOMPUTER IN MONITORING SYSTEM

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980, pp 8-9

[Article by Candidate of Technical Sciences V. V. Sumin and engineers A. G. Vasil'yev and V. N. Syrtsev: "Systems for Processing Ellipsometric Data"]

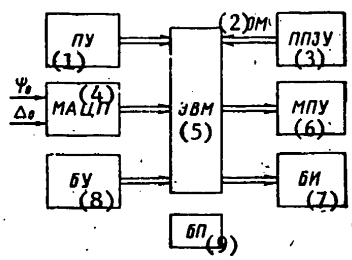
[Text] During the study of the dividing surfaces and boundaries of media, in particular when determining the thickness and optical constants of thin film in the epitaxy-planar technology of manufacturing integrated circuits, the problem arises of processing ellipsometric data. This problem is becoming especially timely under production conditions of manufacturing integrated circuits where output monitoring is organized. In this case two very important requirements are made of the data processing system: (1) the computational equipment must insure operational processing of data and have acceptable dimensions; (2) rapid and accurate computation is essential. These two requirements are to some extent contradictory. This article proposes looking for a compromise solution using an equipment complex based on the domestically produced Elektronika S5-12 single-card microcomputer.

Statement of the Problem

The processing of ellipsometric data involves analyzing the optical parameters of an epitaxy layer (in our case the film thickness d and the index of refraction n_1) according to measured angles of polarization ψ and Δ, which are related by the fundamental equation of ellipsometry. For good-quality operational monitoring of epitaxy films the equation of ellipsometry should be solved with a high level of precision (parameter d with a precision up to 10^{-10} meters, parameter n_1 with an absolute error of 0.01) and speed (for each measurement of angles ψ and Δ the output parameters d and n_1 are determined; the cycle between measurements is five seconds). The use of generally accepted gradient methods of solving nonlinear equations without special software makes it possible to receive the required characteristics of the computational process only thanks to the employment of highly productive general-purpose computers of the BESM-6 type. The development of special computing measures oriented to the use of low-productivity microcomputers is a serious problem, some aspects of whose solution are presented in this article.

Structure of the Equipment Complex

The problem posed of processing ellipsometric data is solved on a hardware complex based on an Elektronika S5-12 microcomputer (see figure). The control



Key:
(1) Printer;
(2) General Mainline of Microcomputer;
(3) Elektronika P5-PPZU Semipermanent Memory Unit;
(4) Multichannel Alphanumeric Printer;
(5) Computer;
(6) MPU16-2 Small Printer;
(7) Indicator Block;
(8) Settings Block;
(9) Power Supply Block.

Structural Diagram of Hardware Complex

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console is designed to turn on the system, check its working condition, put it in a work regime, and prepare to process the next measurement. The multichannel alphanumeric printer makes it possible to feed data on increments of the angles (ψ_0 and Δ_0) in sequence to the digital channel of the computer. The settings block stores the values of the constant components of the measurement (ψ_y, Δ_y, and so on) which can be fed to the computer at any moment; during the input process the parameters $\psi = \psi_0 + \psi_y$; $\Delta = \Delta_0 + \Delta_y$.

The following requirements were made of the structure of the complex: minimize the number of nonseries control assemblies and organs; insure visual monitoring of parameters; document the measurement made and compute the parameters. For this reason when external equipment is connected into the complex the direct linkages of the contacts of the peripheral device predominate — the bit position of the digital channel of the computer while the data conversion functions are assigned to the computer. In addition, the complex has two other characteristics: the deficit of digital outputs is eliminated by the use of dynamic indication and the microcomputer works in a start-stop mode (using the signal "sozh") in the print cycle.

The base computer in the complex is an Elektronika S5-12 microcomputer. This model of microcomputer was chosen on the basis of the following considerations.

The Elektronika S5-12 is a single-card machine built into the technological equipment of the microcomputer and is produced in series by domestic industry. Two models, the Elektronika S5-01 and Elektronika S5-02, are produced for full-scale debugging of algorithms and programs. Multichannel 13-bit reversible alphanumeric printers and other compatible hardware are manufactured for the Elektronika S5 family of microcomputers.

Software of the Complex

The system software for processing ellipsometric data took shape on the basis of solving two major problems: finding a modification of the algorithm for solving the ellipsometric equation with a high speed, and implementing the modified algorithm on the Elektronika S5-12 microcomputer.

The first problem is obviously a classical mathematical problem. Within the framework of this problem it is possible to solve the equation of ellipsometry relative to a parameter (film thickness d); the second parameter (n_1) is found as a value of the variable that insures the minimum for a specially selected criterion (mismatch of the measured and computed values of the parameter).

The second problem is typical for applications of microcomputers that do not have operations with a floating decimal point and operations with double word length. It is apparent that to get maximum speed (that is, minimum time required to solve the ellipsometric equation) a microcomputer mode with a fixed decimal point should be selected as the primary mode. In this case, however, to attain the assigned precision the computing algorithm must be subjected to careful analysis to study the nature of the distribution of error during computation and establish "tight" spots in the procedure where the loss of precision is most significant. Errors of the following types are greatest: constraint error that arises because of the limited length of the computer word format; error in methods of executing fragments of the computation (subtracting proximate numbers, division by small numbers, and the like); raw data error.

It is practically impossible to obtain analytic estimates for the values of these types of error in such complex computing procedures. Therefore, it is more convenient to make a preliminary estimate of precision by modeling the computing procedure on a general-purpose minicomputer with the approximation of results characteristic of a microcomputer with a 16-bit word length. To do this the entire computing procedure for determining parameters d and n_1 of the epitaxy layer is broken into fragments. Each of them is given by a series of possible computation structures which have their own total error values, and after modeling the chain of fragments that provides the least resulting error is selected. The scaling places in the processing program and the processing places are established analogously with doubled precision for each specific computation problem. Debugging and aggregating of programs were done with a complex of a Nairi-K computer, and Elektronika S5-12, and a Videoton 340 display, as well as on an Elektronika S5-01 microcomputer.

During construction of the system for processing elliptometric data on the basis of the domestically produced Elektronika S5-12 microcomputer the possibility was established of using a single-plate microcomputer of the Elektronika S5 family of the first technological generation as the processing means in the stage of operational monitoring of the two principal parameters of an epitaxy layer. At the present time, a model of the processing system has been built and comprehensive debugging of working programs for the Elektronika S5-12 microcomputer is being completed. The more productive Elektronika 60 model microcomputer should be used to get higher indicators of processing quality (speed and precision).

[72-1176]

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CSO: 1863

UDC 681.323

GENERAL-PURPOSE COMPUTER COMMUNICATIONS SYSTEM UTILIZING ELEKTRONIKA-60

Moscow VYCHISLITEL'NYYE SREDSTVA V TEKHNIKE I SISTEMAKH SVYAZI in Russian No 5, 1980 pp 71-79

[Article by I. A. Mamzelev, M. Yu. Artem'yev, K. G. Knyazev, and V. N. Kudryashov: "General-Purpose Computer Communications System"]

[Text] It is possible to identify a large number of problems in contemporary communications engineering requiring computers for solution, for example various scientific-technical calculations, economic problems, tasks performed by an automated system for communications control, the jobs of controlling switching centers, and the like. Thus, virtually all the primary functions of processing, storing, and distributing digital information are formed with computers, and for different jobs computers with different parameters will be required, from microcomputers to highly productive computing systems.

It seems wise to devise a certain basic general-purpose computer communications system for the communications sector. This would be a system of broad application that meets all the needs of the sector for computer equipment. In conformity with the tasks that are performed, the structural principles of the general-purpose computer communications system should meet the following requirements:

1. The system should be composed of modules and capable of being built up. This makes it possible to use similar modules to put together computing devices to solve problems of varying degrees of complexity;

2. The number of types of modules should be minimized with a high degree of repetition among them. In this case it is possible to build inexpensive computer equipment because the primary requirement of microelectronics is met: mass production of a limited assortment;

3. The already-developed software of the system module should be used as the nucleus of the software of the general-purpose computer communications system;

4. The general-purpose computer communications system should guarantee improved computational reliability and be able to function when some of the equipment is down.

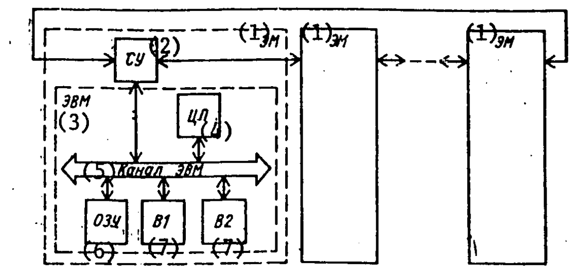
The homogeneous computing systems constructed on the basis of a model of a collective of computers meet these requirements fully [1]. In this case the general-purpose computer communications system is a set of identical elementary machines interlinked in the standard manner. Each elementary machine includes a general-purpose base computer and a system unit which provides communications between this elementary machine and neighboring ones and carries on interaction within the machine [1, 2]. The elementary machine is a module of the general-purpose computer communications system.

This general-purpose system allows easy adaptation to the necessary class of problems: the number of elementary machines in the system can be changed by connecting or disconnecting certain machines. The total number of elementary machines in the system is unlimited. The productivity of a system of K elementary machines when solving one complex problem in the system increases proportional to the number K. It is also possible to use an individual elementary machine of the system in a self-contained mode, which may be required for simple problems. The general-purpose system has improved reliability; when an individual elementary machine goes down, the remaining ones continue to solve the problem after reorganization.

It is advisable to use one of the existing microcomputers built on the basis of large integrated circuit technology as the base general-purpose computer. This reduces the time for development of the general-purpose computer communications system and makes it possible to use existing software. In addition, the use of microcomputers makes it possible to build large systems (several dozen machines) without being seriously limited by the dimensions of the device and the power input. Below we will consider one alternative of hardware for a general-purpose computer communications system that uses Elektronika-60 microcomputers, which have very broad capabilities.

We will consider the principal characteristics of the Elektronika-60 computer that are important from the standpoint of the system. The structure of the computer is shown in Figure 1 below. The figure indicates that the computer is constructed on the modular principle, that is, all functional blocks have the form of completed design units (modules) and communication among them is carried on through a single data exchange channel (single-coupling interface). The principal modules are the central processor (ЦП), the memory modules (ОЗУ) with 4,000 16-bit words each, and the modules of the data input and output unit (B1, B2). The computer channel provides communication among two units interacting on the "active-passive" principle at any moment. The active unit (in Figure 1 the central processor) initiates an access cycle to the channel in conformity with the working program, meets interrupt requirements, and monitors the direct access to memory. Communication is carried on through the channel by the "handshaking" method. The computer has a speed of 250,000 ops per second when performing register addition.

One of the key problems facing the developers of general-purpose computer communications system is the problem of choosing the structure of the system,



Key:
(1) Elementary Machine;
(2) System Unit;
(3) Computer;
(4) Central Processor;
(5) Computer Channel;
(6) Memory Unit;
(7) Input-Output Unit.

Figure 1

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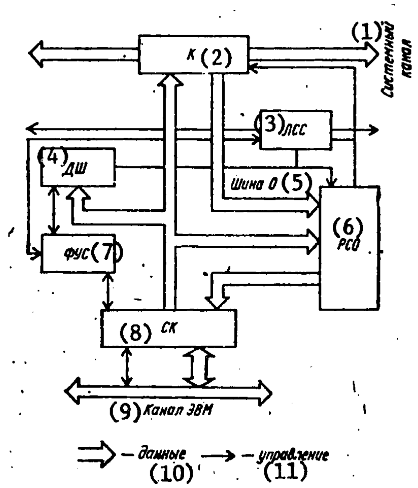
that is, how to interlink the elementary machines (the term "macrostructure" is used). The macrostructure should provide maximum values for the indicators of survivability and switchability and minimal delays during transit data transmissions among the elementary machines. In addition, it should permit simple change in the number of elementary machines without alteration of the hardware and significant changes in the software of each particular elementary machine. These requirements are met by standard P_n machine linkages; each elementary machine is connected to its two neighboring machines by each of k coordinate axes (a k-dimensional cube). In existing systems k is small (k = 1 for a circular system or k = 2 for a lattice structure) because the intricacy of the system unit increases sharply for large values of k. Circular structure was chosen for the general-purpose system we are considering. This decision made it possible to meet the basic requirements made of the structure of the system with fairly simple realization of the system unit (the entire unit can be put on a standard Elektronika-60 computer plate).

The system unit that was developed can increase the number of microcomputers in the system by simply connecting in new computers to those already existing (through the system unit); break the system into independent functional subsystems by programmed control; reorganize the configuration of the system by programs; destroy old and form new subsystems applicable to the problems being solved; exchange data among computers of the subsystem in the process of jointly solving one complex problem.

Figure 2 below is a schematic diagram of the system unit. In conformity with the general principle of functioning of the Elektronika-60 computer the system unit is connected to the computer channel as an external unit. The main functional blocks of the system unit are: the block of registers of systems operations (PCO) by which system interactions are accomplished; the program-controlled commutator (K) of communications channels with neighboring elementary machines; the control signal shaper (ФУС) for the computer channel; the block of system signal logic (ЛСС) which produces system control signals in conformity with the operation algorithm of the general-purpose computer communications system; the decoder of addresses (ДШ) which the central processor of the particular elementary machine uses for access (in cases determined by the algorithm it produces the required functional signals); the coupling block (CK) with the computer channel. It is designed to meet the electrical demands of the channel for user devices.



Key:
(1) System Channel;
(2) Commutator;
(3) System Logic Signal Block;
(4) Address Decoder;
(5) Line 0;
(6) Block of System Operations Registers;
(7) Control Signal Shaper;
(8) Coupling Block;
(9) Computer Channel;
(10) Data;
(11) Control

Figure 2

As theoretical research and experience with construction of the first homogeneous computing systems demonstrated [2, 3, 4], there are four system operations that must be realized to insure the functional integrity of the system (that is, to insure the possibility of joint solution of one complex problem by several elementary machines). These are: adjustment, exchange, system synchronization, and generalized unconditional branching.

Various features of the structure and architecture of the Elektronika-60 require a specific approach to the system unit. Thus, it is not possible to supplement the computer command system with commands for interaction within a machine, which insures most rapid performance of these interactions (as was done, for example, in the Minsk-222 system [3]), because the microprogram control of the computer is closed. To make it possible for the computer to work in the general-purpose computer communications system the computer software is supplemented by an expanded operations system that makes it possible to carry out system interactions. The computer operations system expanded by a set of system programs is the primary operations system of the base elementary machine.

A group of program-accessible functional system operation registers was included in the composition of the system unit for the proposed general-purpose system to accomplish system interactions. The functional characteristic of the registers means that one register corresponds to each system operation: the adjustment register; the exchange register; the system synchronization register (trigger); the generalized unconditional branching register. The

Elektronika-60 uses the following principle to address external units: each external unit contains one or several registers which is assigned a fixed address from the address field of 4,000 higher-order words of memory. In conformity with this principle, a fixed address is given to each system operation register; the address decoder "remembers" these addresses. Reference by the central processor to a definite address signifies performance of the system operation corresponding to this address by the particular elementary machine. There are also two service registers: the current state register (PTC) and the state of the unit register. Their purposes will be described below.

Let us consider system interactions in the general-purpose computer communications system.

1. Subsystem adjustment. Adjustment is the first stage in performing a difficult problem. The subsystem designed to perform this problem is shaped in this stage. Adjustment of the entire subsystem is accomplished from the elementary machine which received the problem (we will call it the controller). The subsystem is a group of elementary machines interlinked by a single system communications channel. Thus, the controller's job is to assign a switching system in its own system unit and then in the system units of the neighboring elementary machines so that all of the elementary machines of the subsystem are interlinked and connections with other elementary machines are cut off.

The type of switching in the commutator is determined by the content of the adjustment register. By feeding the appropriate data to the adjustment register it is possible to obtain the following switching alternatives: linkage only with the neighboring elementary machine to the right (left); linkage with both neighboring elementary machines and transit data transmission through the system unit (full linkage); full breaking of switching. Each transit elementary machine of the subsystem is adjusted by the controller to full linkage, while the extreme left (right) machine of the subsystem is adjusted for linkage with its right (left) neighbor.

The controller uses a specially allocated fictitious adjustment address for issuing the adjustment word to neighboring elementary machines. When the decoder recognizes this address it sends the adjustment word from the computer channel not to the adjustment register, but to the data line of the system channel in the direction assigned by the commutator. A special control line (each system operation has its own line) is used in the system channel to identify adjustment information. To control the identification signal the adjustment word goes along line 0 of the receiving machine to the adjustment register. At the same time the identification signal (not only for adjustment but also for other system interactions) arrives at the control signal shaping block. It causes an interruption of computer work and entry of the code "1" in the position of the current state register corresponding to adjustment (the other three positions of the current state register perform the same functions for the other three system operations).

Any interrupt from the system channel causes the computer to refer to a special program, the supervisor of system interactions, which is included in the operations system of each base elementary machine. The supervisor analyzes the positions of the current state register in order, finds the position in which the code "1" is entered, and executes the subroutine corresponding to the system operation being performed. For adjustment the machine executes system synchronization (see below) and upon emergence from the interrupt begins execution of its branch of the special-purpose parallel program.

The adjustment subroutine of the subsystem is part of the operations system of each elementary machine. This subroutine may be stored permanently in the memory unit or kept on an external medium and called into memory only when the particular elementary machine receives a complex problem.

2. Exchange. As analysis demonstrates [1], the broad multiplicity of exchange interactions can be reduced to the following types: translation exchange (one elementary machine transmits and the others receive); conveyor exchange (all elementary machines of the subsystem form a circuit in which each machine receives data from the preceding one and transmits it to the next); paired exchange (only two of the elementary machines of the subsystem are interlinked); collector exchange (one of the elementary machines of the subsystem collects information from all the others). It is not possible, however, to accomplish all these types of exchange by hardware because they have functional redundancy.

It has been theoretically shown [5] that all these types of exchange can be accomplished by just one translation exchange. In addition, in practically 70 percent of the known problems it is translation exchange that the system needs. The other types of exchange can be accomplished by software. For these reasons only translation exchange was accomplished by hardware in the system we are describing. Any of the elementary machines of the system is able to ignore exchange information by entering the program code "1" in the appropriate position of the system register.

During exchange the transmitting elementary machine copies the exchange word according to the address of the exchange register. The decoder block recognizes the exchange register address and produces a functional signal to accompany information along the system channel. The exchange data itself goes directly to the data line of the system channel. In each of the receiving elementary machines data from the system channel under the control of the escort signal is stored in the exchange register. The escort signal, as was also true for the adjustment signal, causes reference to the supervisor of system interactions which reads data from the exchange register at the address determined by the special-purpose program.

3. System synchronization. This is always done before system interactions because the lengths of the branches of the parallel program in an elementary machine of the subsystem may differ and before exchanges it is essential to be sure that all elementary machines of the subsystem have already completed their segments. This operation is also done immediately after adjustment.

The elementary machine which is performing the synchronization enters the code "1" in the current state register by program. When all the elementary machines of the subsystem have performed the synchronization, the system logic signal circuits produce a generalized character, the signal of system synchronization. It goes to all the elementary machines of the subsystem by a special wire of the control line of the system channel and is processed in a way similar to the signals that accompany adjustment and exchange. The supervisor of system interactions requested by the systems synchronization signal clears the current state register to "0" and continues execution of its branch of the special-purpose program.

4. Generalized unconditional transfer. This system operation makes it possible to modify the course of computation in all elementary machines of the subsystem from one controlling elementary machine, not necessarily the controller. Generalized unconditional transfer is realized in a manner similar to that of the exchange operation. The only difference is that the supervisor of system interactions, after identifying the generalized unconditional transfer, performs an unconditional transfer in its own elementary machine, that is, it loads the command counter from the cell whose address is determined by the content of the exchange register.

The supervisor of system interactions which, with the system unit hardware, executes the above-described interactions within the machine is a part of the software of the general-purpose computer communications system. It consists of two parts: the software of the base Elektronika-60 computer and the system software. In addition to the supervisor of system interactions the system software includes a set of control programs that organize the functioning of the general-purpose computer communications system as a single system.

Let us consider several important aspects of use of the general-purpose computer communications system.

1. Parallel programming. The problem of writing parallel programs for the proposed general-purpose system can be done either manually or using an automatic unit for breaking programs into parallel parts and cross-translators based on large computers. This is because the Elektronika-60 does not now have adequate memory volume to store parallel translators. Later, as the assortment and capacity of peripheral units expands, the paralleling functions can be assigned to the controlling elementary machine itself.

2. Loading a parallel program in the system. In the simplest case the branches of the parallel program can be loaded separately in each of the elementary machines of the subsystem. However, this solution is too labor-intensive and unreliable. Therefore, at the present time the computer assembler language is expanded with operators that describe the parallel features of the program. The program is fed to the controller in the language of the parallel assembler, after which all functions related to translation and adjustment of the subsystem and distribution of branches are performed by the operations system of the controller.

3. Monitoring and diagnosis. If one of the elementary machines of the subsystem goes down during the process of solving a complex problem the controller refers to the reconfiguration programs that are part of the operations system of the base elementary machine. After reorganization of the configuration either a new subsystem is formed or the branches of the parallel program are redistributed among working elementary machines. As a result, problem

solving continues, although at a slower speed. Where reorganization of the configuration is not possible, the controller stops the problem-solving process and prints out an appropriate message, switching to diagnostic programs. The ability to reorganize the configuration makes the general-purpose computer communications system more reliable and gives it greater survivability than an individual computer.

4. Specialization. It is possible to specialize the general-purpose computer communications system in solving particular problems, for example the problem of controlling the switching center. In this case the system of commands of the base computer can be supplemented by installing large integrated circuits of permanent memory with microprograms for performance of user commands on the panel of the central processor. The peripheral equipment can be connected to the computer channels through appropriate controllers.

In conclusion we will note that the principles on which the general-purpose computer communications system we have described was built may also be used to build such systems with other types of structure, for example matrix structure.

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[74-11176]

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RECOGNITION OF GRAPHIC AND SOUND SIGNALS

Kiev RASPOZNAVANIYE GRAFICHESKIKH I ZVUKOVYKH SIGNALOV in Russian 1979 signed to press 28 Nov 79 pp 2, 101, 71-81

[Annotation, table of contents and excerpts from collection of papers, Kiev Institute of Cybernetics, 400 copies, 105 pages]

[Text] New results are presented in the area of the automatic understanding of continuous speech, of the statistical theory of recognition and of the economical assignment of great numbers of images and speech signals by means of grammars. A description is given of a complex of programs for analyzing and recognizing voice signals, of an algorithm for determining the poles of a voice signal in real time, of experiments on the recognition of difficult-to-distinguish machine-written characters, and of comparative results of using various methods of analogy in the area of the recognition of sound signals and images.

CONTENTS

UDC 621.391:534.4:681.3.06:51

Vintsyuk, T.K., Gavrilyuk, O.N., Kulyas, A.I. and Shinkazh, A.G.

Complex of Programs for Processing and Recognizing Voice Signals

A system for the phoneme-by-phoneme recognition of speech has been in operation since 1973 at the Ukrainian SSR Academy of Sciences Institute of Cybernetics. Training and speech recognition algorithms form the basis of the system's problem-oriented software. The complex of programs realizing these algorithms includes programs for preliminary processing of the voice signal, for training and supplementary training, and for the recognition of individually pronounceable words and phrases run together. These basic programs are used together with systems programs for input-output of a voice signal and for displaying the results of recognition on a lit display. The structure of the program complex is illustrated in the figure [not reproduced]. The system has been created on the basis of the BESM-6 computer.

The complete training process for a dictionary numbering 200 words with a five-time pronunciation of each word requires about four hours of machine time on the BESM-6.

Twenty-two K bytes are required for storing in the computer's main memory an SFI [standard data file] designed for the recognition of 500 words. Twelve K bytes of memory are required for producing a primary description of a voice signal two seconds long.

The duration of operation of the recognition algorithm is approximately proportional to the size of the dictionary used at a given moment as well as to the length of the realization of the word to be recognized. A one-second realization of a word is recognized in 0.4 s with a dictionary with a size of $K = 50$ words, in 0.8 s with $K = 100$, in 2 s with $K = 200$ and in 7 s with $K = 500$. For producing a primary description of the one-second realization of a voice signal 0.3 s is required. Thus, if the size of the dictionary equals $K < 100$, the recognition of individually pronounceable speech words with a BESM-6 computer is performed practically in real time. The result is displayed in text form on the computer's display panel.

The reliability of the recognition of individually pronounceable words equals 98 percent for a dictionary of 500 words and 96 percent for a dictionary of 1000 words. In the recognition of continuous speech from a dictionary of 200 words three percent of errors was produced for words in phrases and seven percent of failures in the recognition of individual words in phrases.

The programs are written in FORTRAN and MADLEN.

The parameters of the system for the phoneme-by-phoneme recognition of speech are such that it can be implemented with mini- or microcomputers with a speed on the order of one million operations of the summation type per second and a main memory on the order of 64 K bytes.

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RAMAN SPECTROMETER CONTROLLED BY AN ELEKTRONIKA-100I MINI-COMPUTER

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 46-51

[Article by V. A. Gaysler, E. Ye. Dagman, A. R. Keyayn and A. S. Terskov, Novosibirsk]

[Excerpts] In the present work a typical application of computers in spectroscopy is examined--the separation of signal from noise.

An installation is described which enables optimizing in real time the process of measurement of Raman scattering, one created on the basis of the DFS-24 monochromator, the Elektronika-100I mini-computer, a photon counting system and a coupling and control unit, realized with use of principles and designs of the CAMAC standard.

Shown on Figures 2 and 3 are a structural diagram and voltage diagrams which explain the working principle of the installation. Figure 4 presents an algorithm for control of data collection and of the installation as a whole. The sample to be investigated is irradiated by a laser beam modulated in intensity. The component of scattered light separated by the monochromator impinges on a photoelectronic multiplier. We used the FEU-79, cooled by liquid nitrogen vapors.

The described installation was used by us to investigate little-studied weak Raman lines in HgI_2. Shown on Figure 5 is a section of the Raman spectrum of HgI_2 excited by a He-Ne laser. The required precision was 10 percent in the experiment.[2] The upper curve was obtained by means of a computer-aided installation. The information accumulation time was 35-40 s in the region of the weak Raman lines of 49, 54 and 64 cm^{-1} and 4 s near the maximum of the strong line 112 cm^{-1}. The lower curve was written manually with a time constant of 10 s (the maximum time constant of photon counting). That integration time, as is evident from the figure, is insufficient for reliable detection of weak Raman lines. In the region of the maximum of the line 112 cm^{-1} the integration time is excessive.

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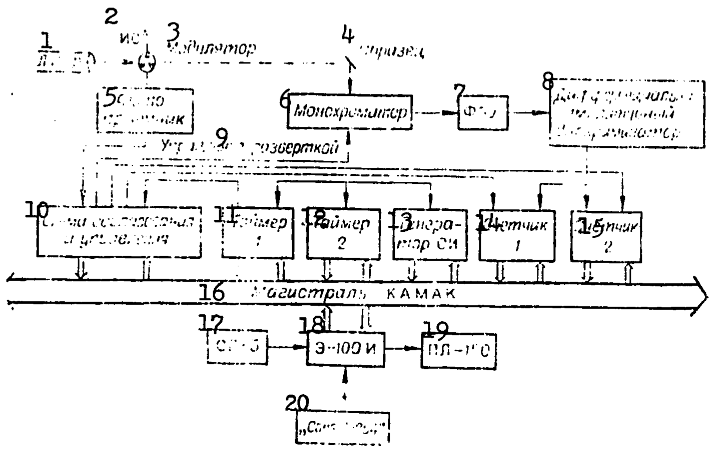

Figure 2. Structural diagram of the installation

1 -- Laser
2 -- Integrated circuit
3 -- Modulator
4 -- Sample
5 -- Photoreceiver
6 -- Monochromator
7 -- Photoelectronic multiplier
8 -- Differential-amplitude discriminator
9 -- Time base control
10 -- Matching and control circuit
11 -- Timer 1
12 -- Timer 2
13 -- SI generator
14 -- Counter 1
15 -- Counter 2
16 -- CAMAC main line
17 -- SP-3
18 -- E-100I
19 -- PL-150
20 -- Consul-254

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ELEKTRONIKA-60 CAMAC SYSTEM

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 42-46

[Article by M. N. Bukharov, V. M. Bukolikov, A. N. Bystavkin, A. Ya. Oleynikov, L. Z. Pososhenko, V. N. Strel'nikov, V. A. Timofeyev and N. A. Tikhomirov, Moscow]

[Text] At present a number of directions are being intensively developed in the areas of physics, geophysics and other areas of science connected with investigations of radio wave propagation, and also with the use of methods of radiophysics to study the properties of the environment. A characteristic feature of such investigations is growth of the role of radiophysical experiments which, as a rule, are conducted in expeditionary conditions. A distinctive feature of expeditionary radiophysical experiments is the need to register and process large volumes of information. Until recently, most often in the course of expeditionary radiophysical experiments the information from the measurement converter outputs was registered on different carriers (mainly in analog form) and the conversion into digital form and processing on a computer were accomplished in stationary computer centers. The effectiveness of investigations in such cases has proven to be low in view of the impossibility of rapid analysis of data and regulation on the basis of its results of the conditions under which expeditionary radiophysical experiments are conducted, and also technical and programming difficulties in data input into the computer for processing.

To intensify and increase the effectiveness of expeditionary radiophysical experiments it is necessary to provide investigators with the possibility of accomplishing directly under expeditionary conditions some types of preliminary processing and maximally simplifying operations on further data processing.

The present work has the goal of developing a standardized system suitable for the automation of a broad class of expeditionary radiophysical experiments. To achieve that goal, in the first stage the task of determining the characteristic requirements for such a system has been set. It is evident that the specifics of expeditionary radiophysical experiments advance as the most important requirements from the point of view of operation of the system those of compactness, small weight, low power consumption and simplicity of servicing. No provision was made for satisfaction of special requirements for work in special expeditionary conditions (high air humidity and temperature, level of vibrations, etc), as most investigations toward which the described developments are directed are done in conditions close to those in the laboratory.

To determine the functional possibilities of the system, an analysis was made of 11 fairly varied expeditionary radiophysical experiments. The results of the analysis are summed up in the table. In explanation, let us note the following. The rates of arrival of information were considered by starting from the requirements for precision of approximation of continuous signals by discrete selections. The volumes of information were estimated from the maximum experimental cycle length (in various cases, the latter amounts to fractions of a second to days). By primary processing is understood processing under expeditionary conditions. It can be accomplished both on a real time scale and in the intervals between cycles (operative processing). The requirement of secondary processing of registered information actually means a need to accomplish registration in a form permitting information input into fairly powerful computers (of the class of the M-4030, YeS-1030, etc) at stationary computer centers.

Starting from the results of analysis, one can readily formulate the requirements for the system and synthesize a standardized structure on the basis of which it seems possible to automate expeditionary radiophysical experiments of a broad range.

If we take into account the principal types of data processing under expeditionary conditions (see table, expt 10), we can conclude that the system must include a digital calculator with a main store with a capacity of over 4 Kbytes and a fairly well developed software. (The requirement for the main storage capacity flows, in particular, from the need to accomplish statistical treatment of the type of calculation of slightly shifted energy spectrum estimates.) It is most advisable now to use the "Elektronika-60" small computer as such a calculator [1].

It is evident that input analog signals from several sources in a system must be converted into digital form. Therefore it is necessary to introduce an analog-digital converter and an analog-signal commutator into the structure of the system. In view of the fact that in the main the data processing is statistical, the maximum reduced value of the quantizing error in level must not exceed 0.5-1 percent. Such an error is assured by an analog-digital converter with 7-8 digits. In that case the commutator must have normalized precision characteristics which can be taken into consideration during processing. It is evident from the table (see expt 4) that for analog-digital converters the necessary conversion time is 5-6 microseconds. This is important for rapidly proceeding expeditionary radiophysical experiments (for example, No 4), and also relatively slow expeditionary radiophysical experiments (for example, Nos 8 and 10, where the precision of calculations of cross-correlation functions, obviously, is critical toward relative shifts of selections. Correspondingly the commutator must have a high speed (a commutation frequency of at least 200 kHz).

Another requirement for the system is assuring the possibility of coupling registered data with signals of a single time system. For that, synchronization equipment must be used in the system.

In addition, the system must provide the possibility of registering information with a volume of 16-18 Mbytes per session in the YeS computer format (see table, experiments 5 and 8), for which registration equipment of the type of digital magnetic tape storages are needed.

Results of analysis of a series of expeditionary radiophysical experiments

A Номер п/п	B Число источников информации	C Вид информационного сигнала	D Скорость поступления информации, байт/с	E Объем информации, поступающей за время цикла, Кбайт	F Требуется ли привязка к сигналам СЕВ?	G Требуется ли регистрация всей первичной информации?	H Требуется ли вторичная обработка?	I Требуется ли первичная обработка, ее вид?	J Основные алгоритмы первичной обработки	K Предста
1	4	1 Напряжение постоянного тока	8	700	Нет	2 Нет	2 Нет	3 Да, ОРВ	4 Пересчет значений, Г	5 Печать [illegible]
2	1	6 То же	$20 \cdot 10^3$	1	»	»	»	3 Да, ОО	С	7 Визуал ской фор
3	1	8 Двоичный код	400	35 000	3 Да	»	3 Да	Да, ОРВ	9 Фильтрация, расчет среднего значения	10 Графи
4	3	1 Напряжение постоянного тока	$150 \cdot 10^3$	3	»	3 Да	»	2 Нет	—	
5	4	6 То же	80	600	»	»	»	3 Да, ОРВ	Г, СТ	7 Визуа ской фор
6	6	»	180	15 600	»	»	»	6 То же	СТ	6 То же
7	4	»	450	1620	»	»	2 Нет	3 Да, ОО	Г, СТ	11 Печать 7 графичес
8	2	»	$16 \cdot 10^3$	18 000	»	»	3 Да	6 То же	С, ВКФ	7 Визуа ской фор
9	6	»	$16 \cdot 10^3$	18 000	»	»	»	»	Г, СТ	6 То же
10	22	»	900	16 000	»	»	»	3 Да, ОРВ, ОО	Г, СТ, ВКФ	»
11	4	1 Напряжение постоянного тока, двоичный код 8	500	10	»	»	»	6 То же	12 Функциональное преобразование, Г, СТ	»

A -- Experiment No
B -- Number of information sources
C -- Type of information signal
D -- Information arrival rate, bytes/s
E -- Volume of information arriving per cycle, Kbytes
F -- Is coupling with single-time system signals required?
G -- Is registration of primary information required?
H -- Is secondary processing required? What kind?
I -- Is primary processing required? What kind?
J -- Main primary processing algorithm
K -- Presentation of results

(Continued)

1 -- Direct current voltage
2 -- No 3 -- Yes
4 -- List of values
5 -- Printing of results of processing
6 -- Ditto
7 -- Visualization in graphic form
8 -- Binary code
9 -- Filtration, calculation of mean value
10 -- Graph on automatic recorder
11 -- Printing
12 -- Functional conversion

(Continuation of Table)
OPB -- processing in real time
00 -- operative spectrum processing
Г -- determination of the distribution law, calculation of dispersion and mathematical expectation
BKФ -- calculation of cross-correlation functions
CT -- calculation of current spectrum
C -- calculation

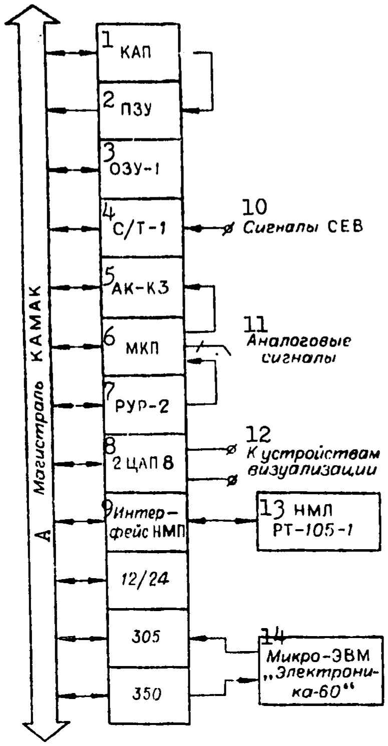
Finally, an important requirement in the system is the possibility of visualization (in graphic and/or alphanumeric form) of the results of processing or the data themselves, obtained in the course of the expeditionary radiophysical experiments. Visualization in graphic form can be accomplished by converting digital data into analog form with the use of a digital-analog converter, with subsequent output to cathode-ray tubes, automatic recorders, etc.

Selected as the basis for realization of the system was a programmable modular CAMAC apparatus, the merits and distinctive features of which are widely known [2].

On the basis of the CAMAC apparatus a standardized system which satisfies the above requirements is readily realized. Needed in that case first of all are the following types of functional modules: rapid analog-digital converters, a commutator, digital-analog converters and a synchronization module. Also necessary is a module for matching magnetic tape stores of a specific type with the CAMAC main line. The possibilities of the system with respect to data processing in real time are greatly expanded if the small computer is maximally relieved of functions of control of data collection and registration. For that purpose the small computer can be connected to the crate through input and output registers and data collection and processing programs are accomplished by the apparatus through use of an autonomous controller and permanent storages [3]. The necessary series of CAMAC-operations is accomplished by the autonomous controller through readout of the corresponding instructions from the permanent storage and their transmission to the CAMAC main line. In that case logical bifurcations and transitions are possible in the algorithm. The organization of that structure thus requires also permanent storage modules, an autonomous controller and input and output registers.

Information can arrive at the visualization device from the calculator's main store. However, often, for example during data output with regeneration to a cathode-ray tube, it is more advantageous to use external storages (a CAMAC module). In addition, such a storage device permits buffering of data during its collection on magnetic tape.

In accordance with these considerations the structure of a standardized system for the automation of expeditionary radiophysical experiments on the basis of the CAMAC apparatus has been developed and an experimental model created (see figure). The realized system is constructed on the basis of a CAMAC crate equipped with sets of modules produced by the Special Design Bureau of the Institute of Radio Engineering and Electronics, USSR Academy of Sciences [4]: (1) an autonomous programmable crate controller, (2) a permanent storage, (3) a storage module, (4) a synchronizer-timer, (5) an analog-digital converter, t_{con} = 2.5 microseconds, 8 bits, (6) a semiconductor commutator (7) a commutator control register, (8) a two-channel digital-analog



A -- CAMAC main line

1 -- autonomous programmable crate controller
2 -- permanent storage
3 -- storage module
4 -- synchronizer-timer
5 -- analog-digital converter
6 -- semiconductor commutator
7 -- commutator control register
8 -- two-channel digital-analog converter
9 -- magnetic tape store interface
10 -- single-time system signals
11 -- analog signals
12 -- to visualization devices
13 -- PT-105-1 magnetic tape store
14 -- "Elektronika-60" small computer

converter, and products of the "Polon" Association (Poland): the 305 (input register), 350 (output register) and 12/24 (auxiliary module to provide the crate main line with a feed voltage of ± 12 V, and also an interface module of a magnetic tape store in model format.

Data are registered on PT-105-1 magnetic tape stores (of Polish origin), which permits recording up to 20 Mbytes on a single magnetic tape in a YeS computer format with a density of 8 or 32 bits/mm.

The great demand for an automation system of the described type makes it necessary to organize its series production.

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NETWORK CONFIGURATION OF COLLECTIVE-USE COMPUTER CENTERS

Riga SETEVAYA ARKHITEKTURA VYCHISLITEL'NYKH TSENTROV KOLLEKTIVNOGO POL'ZOVANIYA in Russian 1980 signed to press 20 May 80 pp 1, 45

[Table of contents from book "Network Configuration of Collective-Use Computer Centers", by Eduard Aleksandrovich Yakubaytis, Institut elektroniki i vychislitel'noy tekhniki AN LatvSSR, 600 copies, 45 pages]

[Text] Contents

[8044/0524-6521]

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CSO: 8044/0524

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Riga SETEVAYA ARKHITEKTURA VYCHISLITEL'NYKH TSENTROV KOLLEKTIVNOGO POL'ZOVANIYA in Russian 1980 signed to press 20 May 80, 45 pages

YAKUBAYTIS, EDUARD ALEKSANDROVICH, Institute of Electronics and Computing Technology, Latvian SSR Academy of Sciences

[Abstract] The standard configuration of collective-use computer centers is compared to the network configuration of these computer centers. The advantages of the network configuration are compared to the disadvantages of the standard configuration. Network configuration provides each user terminal with access to the resources of several operating computers; the load on the communications channels is relieved and the reliability of information processing is enhanced; information can be transmitted among all user stations of the collective-use computer center; there is the possibility of communicating with the resources of other computer centers. A communications system based on the SM-4 minicomputer has been developed and network configuration of collective-use computer centers has been tested. Collective use of the resources of YeS EVS [Unified computer system] and SM EVM [International small computer system] machines and communications channels is highly efficient in the network configuration. Processes related to storage, transmission and processing of information can be changed qualitatively with extensive use of network configuration and a hierarchical state network of computer centers can be developed.
[8044/0524-6521]

EXPERIMENTAL COMPUTER NETWORK OF THE LATVIAN ACADEMY OF SCIENCES

Riga EKSPERIMENTAL'NAYA VYCHISLITEL'NAYA SET' AKADEMII NAUK LATVIYSKOY SSR in Russian 1980

[Article: "Experimental Computer Network of the Latvian Academy of Sciences"]

[Text] The experimental computer network (EVS) of the Academy of Sciences of the Latvian SSR is a multicomputer hierarchical computing association integrating computers specialized with respect to structure and software into a unified system making equipment and software available for the collective use of academy scientists.

The EVS has been created in pursuit of two basic objectives:

1. the conduct of scientific studies in the area of computer network architecture;
2. the construction of a base for an academy-wide system for automating scientific research.

The diagram shows EVS architecture as of October 1980. The logic structure of the computer network comprises two basic types of elements: systems (multilevel, hierarchical groups of programs) and the physical links connecting them. The EVS consists of operating, terminal, dispatching and communication systems. Each one of these is realized in one or in several computers.

The operating systems determine the basic data-handling and computational resources of the EVS. These systems are realized in the YeS [unified system]-1033/1, YeS-1033/2 and YeS-1030-2 computers. The operating system comprises the OS 4.1 standard operating system and the KROS system program, to which are added a logic interface converter and a transport unit.

The KROS program plans the computing operations:

- increases computer productivity;
- automates a number of computer operator functions;
- expands computer capacity (ordering tasks, controls job flow...);
- reduces resource requirements;
- feasibility of remote job input/output.

The logic interface converter makes possible the interaction of operations executed within the YeS EVM [unified computer system] with the network. The transport unit controls the link-up of these operations via virtual (logic) channels of the EVS.

The dispatching system is operated by the set of DISPETCHER 1.7 programs, which:

- controls data flows through local input/output units (printers and key-punch machines);
- receives jobs from terminal-system users;
- converts formats and codes;
- monitors accuracy of incoming data and reinterrogates in case of error;
- buffers messages on magnetic disk in external storage;
- selects the operating system to be used in executing successive jobs and transfers jobs to it;
- stores jobs and results of job execution in external storage;
- transmits results to terminal-system users in delayed or immediate result-output modes;
- stores user files on dispatching-system disks and transfers them to users upon demand;
- collects statistical data on the operation of the computer network;
- distributes jobs among several operating systems performing computational functions.

The dispatching system is used with the YeS-1030/1 computer. In case of failure or repairs, its functions are transferred to the YeS-1030/2 computer. A unit not shown in the diagram performs the switching required in these instances.

The communication systems operate with the SM-3/3 and SM-3/1 minicomputers, the former constituting the operational, the latter the experimental-research node of the communication network. Each system provides execution of the following functions:

- routes packages;
- checks packages following transfer via any physical channel connecting a pair of computers;
- temporarily stores packages in internal storage;
- keeps statistics on node operation and compiles records and documentation.

The dispatching and communication systems establish virtual (logic) channels within the EVS linking operations performed in the operating and terminal systems.

Terminal-system operation is governed by special sets of programs used with the SM-3, SM-4, YeS-1010 and the Wang-2200 minicomputers. Each of these sets provides interactive job preparation, text library maintenance and interaction with YeS EVM system programs.

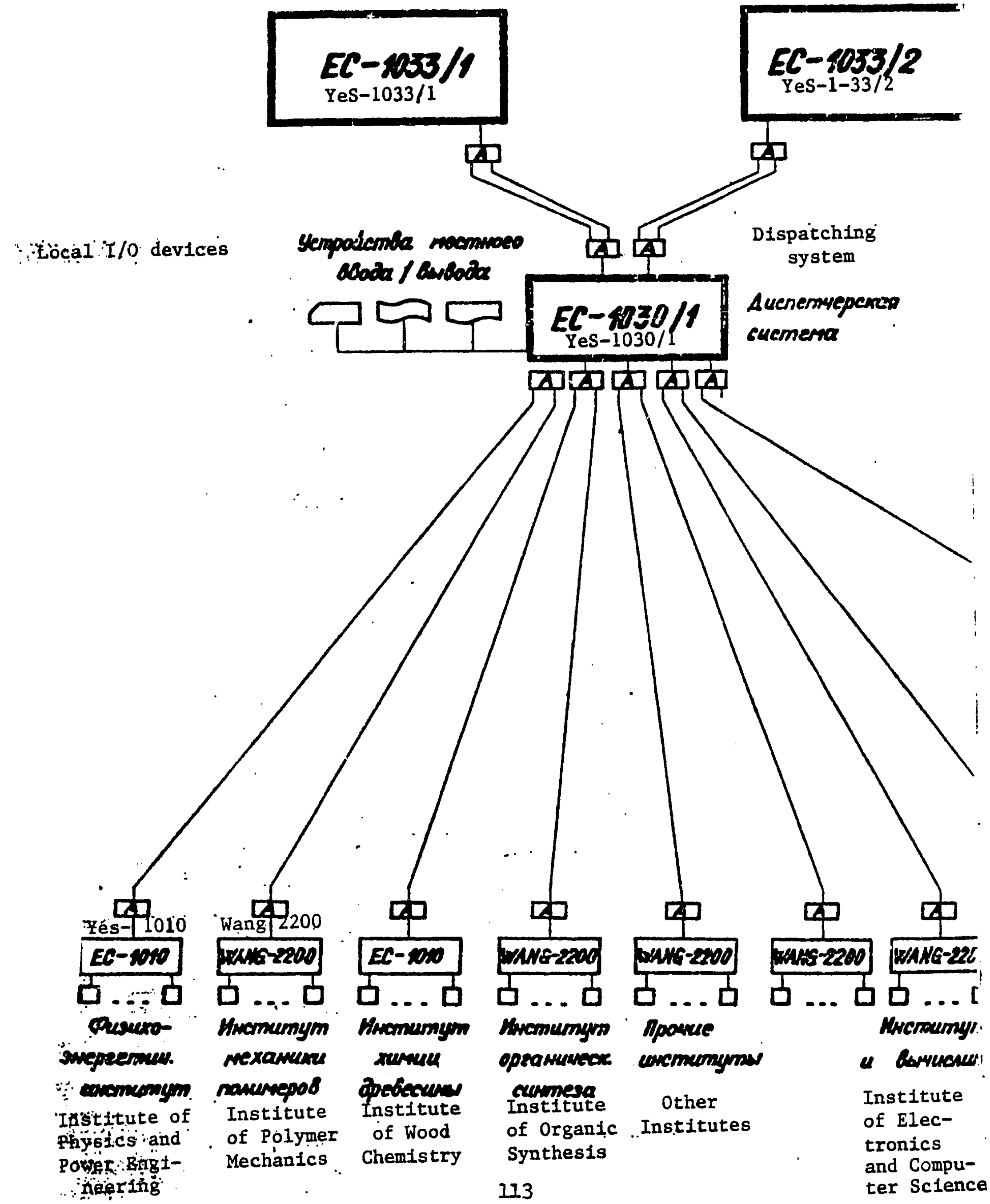
"Data" packages specified by Recommendation X.25, approved by the MKKTT [International Telegraph and Telephone Consultative Committee], provide data exchange between operating and terminal systems. The EVS allocates virtual (logic) channels for this purpose.

Interaction among systems within the EVS is governed by a hierarchy of protocols comprising seven levels: 1 - physical, 2 - channel, 3 - network, 4 - transport, 5 - session, 6 - representational, 7 - application.

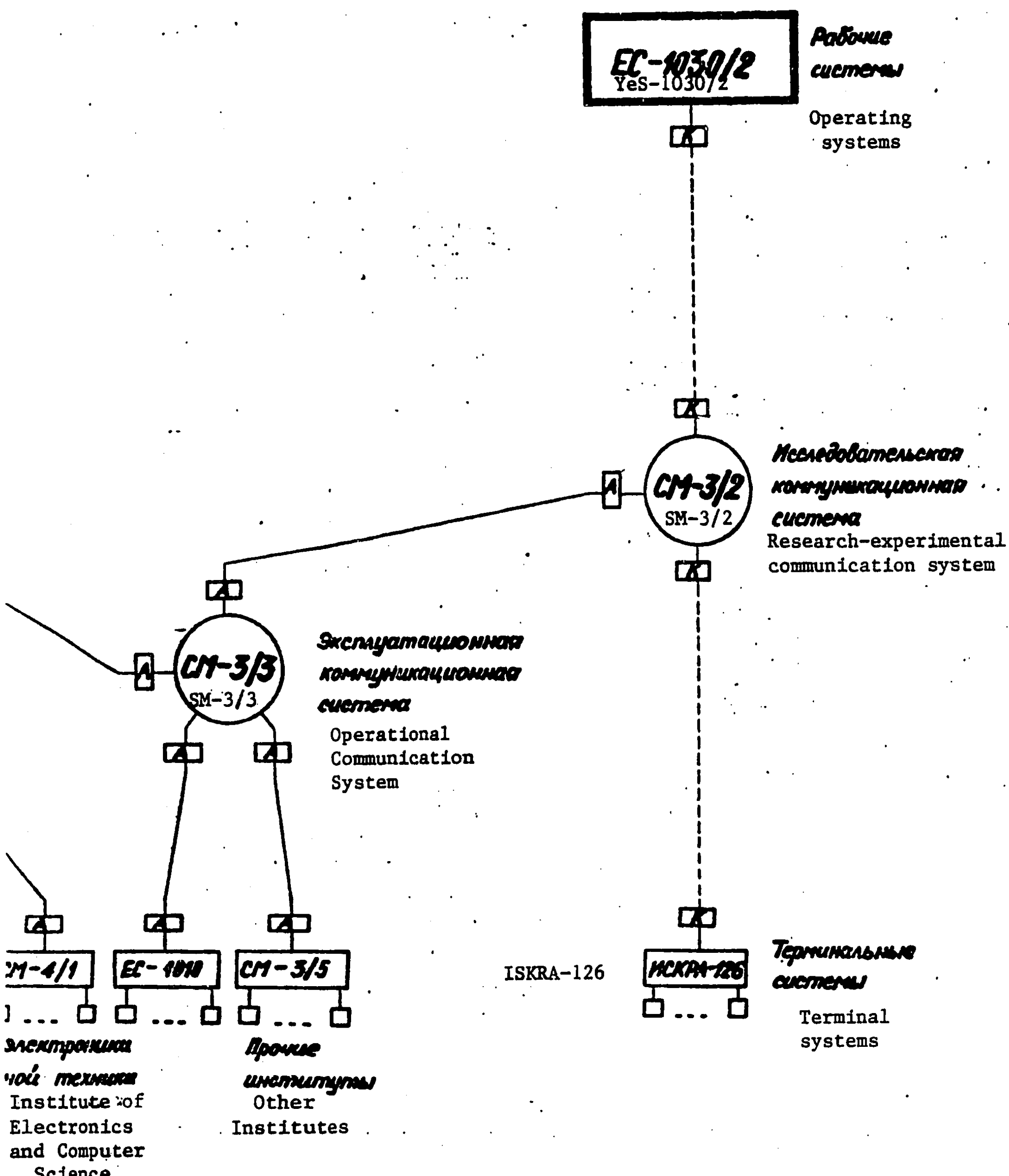
Parallel- (solid lines in the diagram) and series (broken lines)-connected physical channels provide the physical link-ups within the EVS. The parallel channels consist of groups comprising 28 twisted pairs of telephone cable each. The computers are connected with these channels through adapters (A), which provide parallel (9-bit), symmetrical, semiduplex, asynchronous exchange of data between them at rates ranging from 0.2 Mbit/s (to a distance of 2000 m) to 1.5 Mbit/s (to distances of 50 m). The

ЭВС Экспериментальная вычислит...

EVS: Experimental Computer Network of the Latvian Academy of Sciences
(as of October 1980)



а сеть Академии наук Латвийской ССР (по состоянию на октябрь 1980 года)



channels in series are established through telephone communication channels. In accordance with Recommendation X.25, they provide synchronous duplex data exchange at rates of up to 2400 bit/s. All channels are capable of transmitting any type of text employing any method of encoding.

The EVS is a computer network undergoing continuous development making available to subscribers an increasingly broad range of services. The following services were available as of October 1980:

- the formation of text libraries in terminal systems;
- text editing in the conversational mode;
- conversational job preparation in YeS EVM languages (PL-1, FORTRAN, ASSEMBLER, etc.);
- management of local job and output solution libraries;
- storage of any texts in file storage;
- planning for computational operations;
- fully automatic remote job input and solution output;
- availability of user-selected operating systems;
- zero-address job execution;
- solutions stored "until called for;"
- automatic recoding and reformatting of data transferred from one system to another;
- automatic rewriting of data from one medium into another (from YeS EVM computer punched cards onto minicomputer magnetic disks);
- output of information on job and solution flows through the computer network;
- data exchange (electronic post) between operators;
- data output to auxiliary units of operating-, dispatching- or terminal-system hardware (displays, printers, punched-card output etc.).

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SOLUTION OF ECONOMIC PROBLEMS ON ISKRA-/534 MACHINES

Moscow RESHENIYE EKONOMICHESKIKH ZADACH NA MASHINAKH 'ISKRA-524/534' in Russian 1980 (signed to press 18 Jun 80) pp 2-11

[Annotation, foreword and excerpt from chapter 1 of book "Solution of Economic Problems on Iskra-524/534 Machines", by Vladimir Georgiyevich Volkov, David Leont'yevich Lozentsvak and Mansur Alikbirovich Shakirov, Izdatel'stvo "Statistika", 20,000 copies, 216 pages]

[Text] The technical and operational characteristics, programming features and practical examples of using the latest models of domestic and some foreign electronic billing and bookkeeping machines (EFBM) for solution of economic problems are considered in the book.

Intended for specialists in mechanization and automation of accounting in various sectors of the national economy.

Foreword

Adding machine offices, the technical base of which are mainly electromechanical bookkeeping (Askota class 170) and also electromechanical and electronic billing machines (Zoyemtron-382/383), are now functioning in different sectors of the national economy of the USSR along with adding machine stations and computer centers. These machines are used mainly to mechanize bookkeeping and accounting and to issue financial and calculating documentation with simultaneous simple arithmetic processing of them. Manual operations are mainly predominate in the production process when using machines of the given class.

Improving the technology of processing accounting and economic information by means of computer equipment is one of the most important problems faced both by specialists of this field and by developers of various types of computers.

Technical progress in the field of microelectronics, developments of external devices and conversion to the unit-modular principle of design of computer equipment made it possible to develop computers of this class with broader technical and operational capabilities.

A new class of problem-oriented minicomputers--electronic bookkeeping and billing-bookkeeping machines, which have replaced electromechanical bookkeeping and billing machines, has appeared recently in the USSR and abroad. One of the machines of this class is the electronic billing-bookkeeping machine (EFBM) Iskra-524/534.

Information processing on the Iskra-524/534 is based mainly on the principles of the production process of keyboard computers. However, the capabilities of these machines permit one to combine and carry out the main operations in one operating cycle without using intermediate steps.

The main advantages of the Iskra-524/534 compared to machines of the Askota-170 and Zoyemtron-382/383 class are:

the use of input programming language which permits description of the procedure of information processing of primary documents in a form similar to natural form;

the possibility of operational replacement of the programs stored on magnetic cards;

the use of magnetic cards as external storage of the machine;

the use of a greater number of memory registers;

operational input of normative-reference information from the magnetic card into the machine.

Moreover, the distinguishing feature of these machines is the fact that they can be installed and used directly at the locations where information occurs and is used. The efficiency of using them is enhanced significantly in this case because operating expenses are reduced significantly.

This situation requires more efficient organizational forms of using machines of the given class and also a search for new forms of constructing the production processes of information processing which take into account the technical and operational capabilities and features of these machines.

Description, analysis of the technical and operational characteristics, programming features and practical examples of using the electronic billing-bookkeeping machine Iskra-542/534 for solution of various types of accounting problems are presented in the given paper.

It is important to note that the described input programming language for the Iskra-524/534 was developed in subsequent, more improved domestic models of machines of the given class (according to GOST [State standard] 16969-78 "Bookkeeping Computers"). In this regard, development of the input language of the described EFBM facilitates the study of language of the new Soviet Iskra-554 computer.

Brief technical-operational characteristics of the mentioned computer and the Robotron-1720 machine produced in the GDR are also presented in the given paper. Comparison of the characteristics permits the reader to gain an idea of the qualitatively new capacities of this class of machines.

Section 1. Main Characteristics and Rules of Program Development

BRIEF TECHNICAL-OPERATIONAL CHARACTERISTICS OF ISKRA-524/534 EFBM AND OTHER DOMESTIC AND FOREIGN MODELS OF MACHINES OF THIS CLASS

1.1. Designation and Spheres of Application of Iskra-524/534 EFBM

The computers under consideration belong to the class of electronic billing-bookkeeping machines. They are based on a microelectronic (integrated) component base and are small models of bookkeeping machines of the Iskra series.

Unlike the baseline model of the Iskra-524, the Iskra-534 has been additionally outfitted with a tape perforator (type UVL 75/20-1), which permits printout of the corresponding information of punch tape simultaneously with document processing, i.e., the machine can be used in systems with higher level machines.

The Iskra-524/534 machines are oriented mainly toward manual entry of input data. However, there is the capability of input and output of digital information on a magnetic card in these machines.

Both models of EFBM are designed for preliminary processing of documents with a large number of graphs and a significant specific weight of storage operations. These machines are equipped with an alphanumeric printer and may be used to mechanize calculating operations where document processing requires printout of the text, calculations by four arithmetic operations, storage of the results of calculations in registers and automatic printout of the digital input data and results of calculations on columns of the document.

The operational-technical characteristics and capabilities of the Iskra-524/534 permit one to use them for mechanized processing of accounting-economic information in large MSB [Accounting-bookkeeping machines] and small MSS [Machine calculating station] of industrial enterprises of various sectors of the national economy, the VTs [Computer center] of TsSU [Central Statistical Administration] of the USSR, at warehouses and bases of material and technical supply and commerce. Along with this, the Iskra-534 model can also be used in ASU for information processing of primary accounting documentation with simultaneous receipt of a technical carrier--punch tape for subsequent data processing on the computer. Complex use of the Iskra-534 as peripheral equipment with other computers makes it possible to design a data processing system which permits one:

reduce the laboriousness of the perforation process and checking of it, to combine this process with simultaneous development of the corresponding output registers and preliminary arithmetic processing of documents;

to formulate punch-tape entry for computers, which significantly increases the rate of entry;

to carry out preliminary grouping and "compression" of indicators in the required case (as a function of the volumes and deadlines of information being processed at the computer center);

to provide the enterprise with additional data of an operational nature;

to take into account in primary document processing programs the requirements of normative acts.

The characteristic feature of the Iskra-524/534 is also the capability of installing and operating them directly in the services of enterprises. In this case the bookkeeper-accountant can work on them: he can calculate wages (preliminary processing of documents) with storage of data on magnetic cards during the month (for calculation of wages) and by months (for calculating the average wage, information on temporary incapacity and leave payments), can calculate taxes and so on. Using magnetic cards, one can compile a personnel record of the worker, information on distribution of the calculated wage by the calculating accounts (by codes of expenses and contracts) and payment information during the first half of the month and for the month as a whole.

1.2. Configuration, Design Features and Main Technical-Operational Characteristics of the Iskra-524/534

The configuration of these models is shown in Figure 1. The technical-operational characteristics of these machines are presented below.

The central processor (TsUO) provides:

entry and translation of the processing program from the input language to the internal code of the machine and recording of the translated program into the OZU [Internal storage];

reception and recording in the input register of information composed by the operator on the keyboard (10-key);

processing the information entered and stored in the OZU according to a previously entered program and control instructions entered by the operator from the control keyboard;

control of the output devices of the machine for formation of documents determined by the program.

The main assemblies of the TsUO are the OZU and PZU [Read-only memory].

The OZU is made in the form of a structurally complete assembly on ferrite cores and is designed to store data and also document processing programs. Ferrite cores provide retention of information by the OZU in a de-energized state and during switching working voltages on and off. At the same time only a single program can be stored in the OZU. The word format of the OZU is four bits (tetrad), capacity is 1,024 bytes and access time is 1 microsecond.

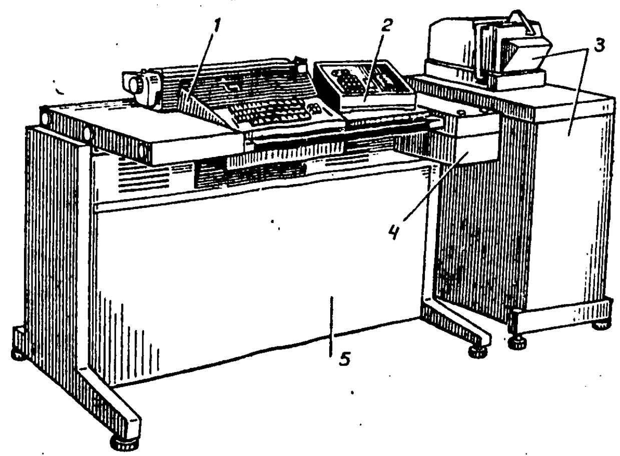

Figure 1. Electronic Billing-Bookkeeping Machine Iskra-524/534: 1--alphanumeric printer (ATsPU); 2--control console; 3--punch tape output device (UVL 75/20-1) with connection of information compatibility device (UIS); 4--recording and readout device from magnetic card (MK); 5--central processor (TsUO) with internal storage (OZU) and read-only memory (PZU)

The transformer type PZU is designed to issue program information by the TsUO which provides interpretation of the input language symbols and microprogram execution of instructions of the document processing program. The capacity of the PZU is 4,096 bytes and access time is not more than 4 microseconds. The PZU is made structurally in the form of a functionally complete assembly.

The magnetic card recording and readout device (UZSMK) (Figure 2) is an electromechanical unit with electronic control and is designed to record (read out) on a magnetic card program information on numerical data arriving in an eight-element code. The UZSMK is made in the form of a device built into the EFBM console.

The information carrier outside the machine is a magnetic card (MK) (Figure 3) with the following main characteristics:

dimensions of 90 X 50.7 mm;

number of information tracks--2;

number of service tracks--1;

number of surfaces for information recording--1;

capability of recording information in two columns. To do this, the MK should be rotated by 180° and inserted with the other end into the device;

the volume of information in one column is 128 bytes;

the speed of the card is 0.2 m/s;

the readout (recording) time of one column of information is no more than 1 second.

The alphanumeric printer (ATsPU) of type Zoyemtron-530 is designed for preliminary entry of the program into the OZU, manual printout of alphanumeric text of the document being processed and automatic printout of input data and the results of calculations. The symbol printer is sequential by using letter levers at a speed up to 10 characters per second. The alphanumeric keyboard of the printer is shown in Figure 4.

The control console (PU) of the machine includes a display, 10-key keyboard (DKV), control keys and is designed to display the status of the machine, to enter input data into it and to start or control the procedure of program execution by the operator (Figure 5).

Technical-Operational Characteristics of Iskra-524/534

Name of Parameters	Value of Parameters
Capacity of OZU for data and program storage	1,024 bytes
Number of programs stored simultaneously in the OZU	1
Format of OZU word	4 bits (1 tetrad)
Maximum digit capacity of entered and retrieved numbers	Variable, up to 12 decimal places with regard to character
Automatic printout and (or) perforation of text (alphanumeric) information	Variable length, only as a text constant of processing program
Number of registers (digital)	Variable, up to 253
Position of decimal in column	Fixed according to program after any decimal point and number of characters after decimal is up to 7
Number of columns in document being processed	Up to 30
Method of installing the printer carriage in the corresponding columns of the document	Automatic--according to program
Printing speed in automatic information output mode	Up to 10 characters per second
Length of carriage platen of ATsPU	460 mm
Maximum number of characters per line	167
Number of different characters printed manually	92
Number of different characters printed automatically	91
Capacity of magnetic card	256 bytes
Speed of automatic output on punch tape	No less than 20 characters per second
Output codes to punch tape:	GOST 130-52-74 With connection of recoding device (UIS), eight additional codes by order of user

Iskra-534	Without UIS, Code GOST 130-52-74 With UIS, Codes GOST 130-52-74, MTK-2 and Minsk-32
Power supply voltage	220 V
Consumed power	300 W
Total mass	Not more than 200 kilograms

The punch card information output device (UVL 75/20-1) provides output of digital and alphanumeric information on a technical carrier in code GOST 130-52-74. The technical speed of perforation is not less than 20 characters per second. Structurally the punch tape output device is made in the form of a separate pedestal and is connected by cable to the central processor. Connection of an additional recoding information compatibility device (UIS) to the perforation unit permits one to print out information in eight additional codes.

[109-6521]

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BRIEFS

OPTICAL MEMORY--Academician Glushkov, director of the Institute of Cybernetics in Kiev, mentions in an interview that in his institute an electron beam can be used to record the information equivalent of the thirty-volume Large Soviet Encyclopedia on an area the size of a matchbox label [Summary] [Moscow OGONEK in Russian No 1, 1981 p 15]

ELORG--The Elektronorgtekhnika All-Union Export-Import Association (Elorg) contains nine specialized firms: Elorg ES - YeS computer exports; Elorg SM - SM computer exports and imports; Elorgsistema - computer system imports; Elorgcomplekt-peripheral device imports; Elorgmash - office equipment exports and imports; Elorgintegral - active components exports and imports; Elorgcomponent - passive components exports and imports; Elorgintech - software exports and imports; and Elorgdetal - maintenance and spare parts exports. Address: SSSR, Moskva, 121200, Smolenskaya-Sennaya pl. 32/34. Telephone: 244-11-19. Telex: 411385. [Excerpts] [Moscow BYULLETEN' INOSTRANNOY KOMMERCHESKOY INFORMATSII in Russian 27 Dec 80 p 4]

LASER COMMUNICATIONS CHANNEL--An experimental laser communications channel, developed by workers of the radio engineering laboratory at Tallinn Polytechnic Institute and operating at a frequency a million times greater than that of television broadcasts, now links Estonian Gosplan and Central Statistical Administration computer centers. [Summary] [Moscow SOVETSKIY VOIN in Russian No 19, 1980 p 26]

REMOVABLE DISK PACK--Academician Glushkov, director of the Institute of Cybernetics in Kiev, has announced that the Elektro Pribor factory has begun serial production of the YeS-5066, a 100M-byte removable disk pack. [Summary] [Moscow PRAVDA in Russian 12 Nov 80 p 6]

BULGARIAN COMPUTERS--The Bulgarian Technical Center of Electronics and Electrical Engineering currently celebrating its third anniversary, is located on Pyatnitskaya Street in Moscow. According to Victor Nikolov, the deputy director, the Center represents the Isotimpex foreign trade association in its sale of computer equipment (in particular, tapes and disks, software and data-preparation devices) to the USSR. The Center tests all computers to be exported to the USSR. Bulgaria's many computer models can be seen in the display hall at the Center. [Summary] [Moscow MOSCOW NEWS in English No 44, 1980 p 6]

BUKHARA COMPUTER CENTER--An oblast computer center has begun operation in Bukhara. A computer capable of performing 800 operations per second has been installed. [Summary] [Tashkent PRAVDA VOSTOKA in Russian 8 Aug 80 p 4]

YeS-1010, YeS-1033 COMPUTERS--The Mangyshlakneft' Association's computer center in the Kazakh SSR is equipped with YeS-1010 and YeS-1033 computers [Summary] [Moscow EKONOMICHESKAYA GAZETA in Russian No 47, 1980 p 15]

[903-P]

CSO: 1863

CONFERENCES, PERSONALITIES

REGIONAL CONFERENCE ON IMAGE PROCESSING AND REMOTE INVESTIGATIONS

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980 p 28

[Announcement]

[Text] The Central Board of Directors and the Novosibirskaya Oblast board of directors of the Scientific-Technical Science of Radio Engineering, Electronics, and Communications imeni A. S. Popov,

The scientific coordinating council on the problem "Aerospace Methods of Investigating Natural Phenomena and Resources" of the Presidium of the Siberian Department of the USSR Academy of Sciences and

The computing center of the Siberian Department of the USSR Academy of Sciences and the Novosibirsk Institute of Engineers of Geodesy, Aerial Photography, and Cartography

Announce

A Regional Conference "Image Processing and Remote Investitation," (OIDI-81), in Novosibirsk, in April 1981.

The conference is being held in conformity with a resolution of the Central Board of Directors of the Scientific-Technical Society of Radio Engineering, Electronics, and Communications and the Presidium of the Siberian Department of the USSR Academy of Sciences. It is proposed to accept reports on the following subjects:

1. Methods and algorithms of processing images for the purposes of preparing them, decoding them, determining coordinates and spectra, and so on (digital, analog, digital-analog).

2. Technical equipment for shaping and processing images: structures and assemblies of optical electronic systems, specialized processors, multiprocessor systems, image input and output units, systems for long-distance image transmission.

Please send report abstracts, up to two pages, in two copies with appropriate documents before 10 December 1980 to the address of the organizing committee, which is as follows: 630008 Novosibirsk, Kirov Street, 86, Oblast Board of Directors of the Scientific Technical Society of Radio Engineering, Electronics, and Communications, OIDI-81.

Telephone numbers for information: 66-03-78, 43-25-66, and 65-02-65.

Organizing Committee

[72-11176]

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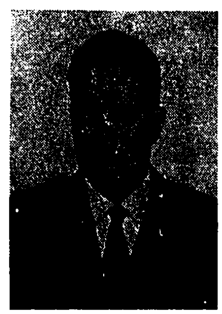
ANNIVERSARY CONGRATULATIONS, CAREER REVIEW OF CONTROL SCIENTIST TRAPEZNIKOV

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 11, 1980 p 17

[Article: "Congratulations to the Celebrant"]

[Text] Hero of Socialist Labor Vadim Aleksandrovich Trapeznikov, academician and outstanding scientist in the field of control problems, is celebrating his 75th birthday.



Vadim Aleksandrovich's first works on control theory go back to the late 1930's, at which time he was a prominent electrical engineer, doctor of technical sciences, and professor. Understanding the importance of production automation for the national economy, Vadim Aleksandrovich devoted his talent and great energy to this new field of engineering, which was in fact taking its first steps. Looking back over his last 40 years of work, we can say confidently that he made a significant contribution to the development of control theory and engineering. If we were to try to identify the most important characteristic of Vadim Aleksandrovich's work, it would unquestionably be his constant desire to relate automation theory organically with practice, with pressing practical needs.

He was one of the first in our country to understand the importance of developing analog computers. Under his direction and with his active participation, the first machine, the EMU-1, was built in the late 1940's at the Institute of Automation and Remote Control (IAT, today the Institute of Control Problems). He was awarded the State Prize of the USSR in 1951 for this work.

Becoming seriously involved with the problems of full production automation, Vladim Aleksandrovich was already proposing broad use of the aggregate-modular principle of building automation equipment in the early 1950's.

In those years IAT and the Tizpribor Plant built one of the first systems implementing this principle, an automated control system for pneumatic instruments. He had an active part in this, and this work played an important rule in creation of the State System of Automation Instruments and Equipment. In the late 1950's he wrote a series of articles proposing the organization of a broad front of work to analyze and insure the reliability of technical articles. These articles stimulated research on this problem in many fields of engineering.

In the early 1960's, under the direction of Vadim Aleksandrovich major multipurpose control systems, the prototypes of contemporary automated control systems for industrial processes, were built. They had such typical subsystems as subsystems for automated monitoring, automatic protection and control in emergency situations, control consoles with means for compression and generalized representation of data to the human operator, and use of logical control means. V. A. Trapeznikov was awarded the State Prize of the USSR for one of the first automated monitoring systems.

In the mid-1960's Vadim Aleksandrovich conducted an extremely timely and original study of the economic aspects of automation. His articles, published in the journal AVTOMATIKA I TELEMEKHANIKA attracted the attention of both technical specialists and economists. In his articles and reports Vadim Aleksandrovich consistently preaches the necessity of establishing economically sound levels of automation and selecting the most efficient tasks of data processing and control for automated control systems.

Vadim Aleksandrovich has devoted much effort to bringing together scientists and practical workers involved with the problems of automation theory and practice. If we can say confidently today that there is a Soviet school of automation, enormous credit for this goes to Vadim Aleksandrovich.

Since the 1950's he has organized and headed what are unquestionably the most prestigious all-Union conferences on control problems. They are held regularly every four years. In addition he has organized symposiums on timely issues of control theory.

For more than 20 years Vadim Aleksandrovich has been head of the National Committee of the Soviet Union on Automatic Control. Under his direction the historic first congress of the IFAK [possibly International Federation of Automatic Control] was organized and held in Moscow in 1960. As first deputy chairman of the USSR State Committee for Science and Technology for 14 years, Vadim Aleksandrovich made a significant contribution to improving the efficiency of scientific research in the country.

The Ministry of Instrument Making, Automation Equipment, and Control Systems, the Central Administration of the Scientific-Technical Organization of the Instrument Making Industry imeni Academician S. I. Vavilov, the editorial board, and editors of the journal wish Vadim Aleksandrovich Trapeznikov good health, creative successes, and inexhaustible energy.

[72-11176]

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CSO:1863

PUBLICATIONS

TRANSLATION OF COMPUTER SECURITY BOOK

Moscow SOVREMENNYYE METODY ZASHCHITY INFORMATSII in Russian 1980

[Summary] This book is a cover-to-cover translation of Lance Hoffman's "Modern Methods for Computer Security and Privacy," which was published in 1977 by Prentice-Hall, Inc.

The work was translated by M. S. Kazarov and M. K. Razmakhnin. The editor is Candidate of Technical Sciences V. A. Gerasimenko.

The translation was published by Sovetskoye Radio in an edition of 12,000 copies.

[128-P]

CSO: 1863

COMPUTER SECURITY AND PROTECTION STRUCTURES

Moscow BEZOPASNOST' EVM I ORGANIZATSIYA IKH ZASHCHITY in Russian 1980 (signed to press 27 Feb 80) pp 4-6

[Annotation and foreword from Russian edition of book "Computer Security and Protection Structures", by Bruce J. Walker and Ian F. Blake, University of Waterloo, Izdatel'stvo "Svyaz'", 5,000 copies, 112 pages]

[Text] The book is devoted to the timely problem of providing the viability of information-computer systems, their security, protection against physical intrusion, qualified penetration to software and also to such random threats as the effect of magnetic fields and breakdowns in equipment operation. Examples of designing protection structures used by IBM and Honeywell companies are given.

The book is intended for engineering and technical personnel specializing in the field of computer center and ASU design.

Foreword to Russian Edition

The development of computer equipment and penetration of it into all spheres of social activity pose problems of providing the reliability of the calculating process to developers and users of computers. The accuracy and timeliness of conducting banking operations, the operational nature and smoothness of transport operation and the rhythm and efficiency of operation of shops and enterprises, energy systems and communications systems now depend on the reliability of hardware and software and also on the reliability of computer system service personnel. If reliability is understood not only as the efficiency of the system but also its security against unsanctioned use of hardware and software and information, then violation of operating reliability may lead not only to significant material losses but to extensive moral losses. Expanding the concept of reliability made it necessary to introduce a new term--computer security. Security is understood in this case as provision of the functional efficiency of the apparatus and of the program and information components of computer systems under conditions of intentional attempts (threats) to disrupt the normal functioning of these components.

The translation of the book of Canadian scientists Professor I. F. Blake and his assistant B. J. Walker, offered to the Soviet reader, is a survey of the current state of the problem of the security of information-computer systems and also measures undertaken to provide security.

The book consists of three parts. In part 1 "Threats," various types of dangers which threaten the system and information as a result of natural events and random and intentional violations of ASU [Automated control system] and VTs [Computer center] functioning, are considered in detail. In Part 2 "Protective Measures," in approaching the problem of protection in a complex manner, the authors describe organizational, apparatus, program and cryptographic methods and means of protection. In Part 3 "Survey of Existing Systems," the principles of designing developed protective systems are described and main attention is devoted to computers of the IBM and Honeywell companies.

Problems devoted to threats inherent to Soviet activity are also considered in the book, but it will be useful for Soviet specialists to become familiar with United States experience in implementation of hardware and software protection.

The material offered in the book together with the extensive bibliography, despite some recapitulation of the outline, permits a wide range of readers to become familiar with the main aspects of threats of security of computer systems and protection structures for them. The book will be interesting to developers, maintenance personnel and users of ASU and VTs

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CSO: 1863

UDC 621.39:681.3

COMPUTER HARDWARE, SOFTWARE FOR COMMUNICATIONS

Moscow VYCHISLITEL'NYYE SREDSTVA V TEKHNIKE I SISTEMAKH SVYAZI in Russian
No 5, 1980 pp 2, 145

[Annotation and table of contents of book "Vychislitel'nyye Sredstva v Tekhnike i Sistemakh Svyazi" (Computer Equipment in Engineering and Communications Systems) edited by S. D. Pashkeyev, Moscow, Svyaz', 1980, 145 pp]

[Excerpts] Annotation

This collection of articles is devoted to current problems of mathematical and simulation modeling by computer of communications equipment and networks, data transmission networks, and message exchange centers. Considerable attention is given to the problems of optimizing models of communications equipment and networks.

The book is intended for scientific workers engaged in designing data transmission networks.

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CSO: 1863

COMPUTING SYSTEMS

Moscow VYCHISLITEL'NYYE SISTEMY, VYPUSK 1 in Russian 1980 signed to press 14 Mar 80 pp 2, 157, 8, 24, 87-88, 94

[Annotation, table of contents and excerpts from book edited by E.V. Yevreinov, Izdatel'stvo "Statistika," 10,000 copies, 160 pages]

[Text] This collection contains new results in the area of the creation of distributed and concentrated computing systems and of their utilization for automating the solution of economic problems in various sectors of the country's national economy. In the articles in this collection are discussed questions of the methodology of designing computing systems and of technological methods of processing economic information by using new computer hardware.

Intended for practical workers, specialists at design organizations, scientific personnel and VUZ students and technical school students.

CONTENTS

Yevreinov, E.V., doctor of technical sciences and professor, USSR Central Statistical Administration VGPTI [All-Union State Design Technology Institute]

The Unified Distributed Computing System; Development Problems and Prospects

Key Steps in and Prospects for the Creation of the YeRVS [Unified Distributed Computing System]

The step-by-step creation of the YeRVS is advisable since it makes it possible more quickly to produce a savings and to make the necessary refinements in the formulation of goals. The creation of the YeRVS can be divided into three steps.

Step 1--the creation of operating models of the YeRVS on the basis of series-produced computer and communications equipment. At this stage it is possible to create distributed computing systems (RVS's) on the basis of third-generation computers, minicomputers and microcomputers. On the basis of the capabilities of the existing production base it is possible to count on designing RVS's with a productivity of 10^7 to 10^8 operations per second. Two or three years are required for designing RVS models.

Step 2--the creation of a distributed computing system for a rayon unit. At this stage it is possible to create a rayon unit RVS from specially developed computer and communications equipment with a productivity of 10^8 to 10^9 operations per second and a specific cost of C_0 (C_0 = 0.1 to 0.01 rubles). Five to seven years are required for this stage.

Step 3--the transition to the mass introduction of rayon distributed computing systems and to their unification into the YeRVS. At this stage the demand of the national economy for computing resources can be satisfied, taking into account the forecasted specific computing capacity, V_g, equal to 10^3 operations per second for 1985, 10^4 operations per second for 1990 and 10^5 operations per second for 2000. Thereby it is possible to achieve a specific cost, C_0, equal to 0.01 to 0.001 rubles.

Selivanov, N.I., USSR Ministry of Communications Central Computing Center, Zhiratkov, V.I., candidate of technical sciences, NETI [expansion unknown], Mishchenko, V.K., candidate of technical sciences, NETI, Mel'nikov, V.I., USSR Central Statistical Administration VGPTI and Kharitonov, V.D., USSR Central Statistical Administration VGPTI

Distributed Computing Systems Based on Second- and Third-Generation Computers

Increasing the productivity of computing equipment involves uniting it into a unified complex. One of these complexes is a distributed computing system (RVS). The key components of a homogeneous computing system are the elementary machine (EM) and the communications system.

Second- and third-generation computers, as well as mini- and microcomputers, are used as EM's.

The communications system in an RVS consists of communications channels and a commutator. Communications channels serve the purpose of exchanging information between the EM's and the Em's and external systems in the process of solving a problem. This exchange can be accomplished in a parallel, serial or mixed (parallel-serial) code. According to the current classification, under the heading of RVS's come systems whose EM's are situated at such a distance that the time required for the propagation of a signal between them is longer than the time for the execution of an operation by the elementary machine. The time required for the exchange of information is determined by the technical characteristics of the computer, the equipment for matching the computer with the communications channel and its utilization. The influence of the exchange time on the productivity of the RVS depends on the degree of coincidence of the processes of computation and of the exchange of information between the system's EM's.

Of all the lines along which RVS's are being developed, two are of special interest: the design of an RVS on the basis of standard and on the basis of specially developed hardware. The structures of RVS's along these lines are discussed in this article.

Distributed Computing Systems Based on Second- and Third-Generation Computers, Designed on the Basis of Standard Hardware

An RVS based on a second-generation computer includes a "Minsk-32," apparatus for matching with the communications channel of the "Minsk-1550 (1560)" type and "Minsk-1500" data transmission equipment (APD).

The selection of this model as the basic one is based on the following:

Interaction between the computer and external equipment by means of a general-purpose communications system (SUS) selector channel.

The transmission of information in parallel code at a rate of 100 K bytes per second.

Intercommunication of the computer by means of control signals through special lines.

The simultaneous performance of four working routines at seven, 10, 11 and 12 levels.

The switching equipment is designed for connecting to the "Minsk-32" the communications channel of a subscriber telegraph network or of local unswitched telegraph lines, as well as APD operating through telephone communications lines.

The equipment makes possible the input and output of information from telegraph and telephone communications lines, as well as the independent operation of each of these lines in the input-output mode.

Distributed Computing Systems Based on Second- and Third-Generation Computers, Designed on the Basis of Special Hardware

The second trend in the design of RVS's consists in the development of special-purpose equipment for linking the computer with communications channels. In the RVS based on the "Minsk-32" was developed a special "computer channel - communications channel" linking unit which in addition to the function of linking also performs certain functions of a systems unit. Several functioning RVS's exist at the present time. The "Astra" linear-structure RVS, consisting of four computers, is being used in Novosibirsk. A linear-structure system consisting of two computers has been introduced at the Ministry of Communications Central Computing Center in Moscow. In 1980 as many as 15 computers will be hooked up to this system. For the first time in practice an attempt has been made to convert the linear structure of the RVS into a ring structure, which improves the reliability and speed of the system as a whole. This is the Ministry of Communications RVS, which must solve the following: complicated problems involved in analyzing and synthesizing electrical and electronic circuits used in communications, radio engineering systems and communications systems; problems associated with queueing systems; problems relating to design work; and problems in servicing a subscriber's network which are specific to the technological work of communications production enterprises. It is precisely the latter class of problems which brought about the use of a distributed computing system for their solution, since experience (e.g., calculations for subscribers for the use of intercity telephone communications) has demonstrated that the employment of a single large-capacity computer does not lead to the total automation of calculations because of an insufficiency of computing capacity.

A linear-structure RVS is described below and its characteristics are given.

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TABLE OF CONTENTS FROM THE JOURNAL 'CYBERNETICS'

Kiev KIBERNETIKA in Russian No 5, 1980 p 149

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ABSTRACTS FROM THE JOURNAL 'PROGRAMMING'

Moscow PROGRAMMIROVANIYE in Russian No 6, 1980 pp 95-96

UDC 681.3.06:51

PARALLEL COMPUTATIONAL PROCESSES AND THE FUNCTIONAL EQUIVALENCE OF OPERATORS

[Abstract of article by Burgin, M.S.]

[Text] The operators for a multidimensional structurally oriented model of parallel computations and multiprocessor systems are studied. Questions of the various representations of the files of the data being processed and the de-paralleling of the calculations and combining of operations are treated. Figures 1; references: 14.

UDC 681.3.06:51

AN AXIOMATIC DESCRIPTION OF CONTEXTUAL LINKS AND CONDITIONS

[Abstract of article by Kritskiy, S.P.]

[Text] A formalized asymptotic definition is proposed for the total syntaxis of programming languages, including contextual links and conditions. A chain is declared permissible if there is a structure among its syntactical structures which is minimal in terms of the selected ratio of the sequence. Questions of computing minimal structures are studied. Figure 3; references: 9.

UDC 519.681

FUNDAMENTALS OF OPTIMAL PROGRAM SYNTHESIS BASED ON COMPUTATIONAL MODELS

[Abstract of article by Val'kovskiy, V.A.]

[Text] A procedure for constructing programs based on a formalized subject area, a computational model, is analyzed. The construction process is broken down into two steps: setting up the computational scheme and the synthesis of the program based on this scheme. The first step can be accompanied by optimization with respect to a number of criteria. Several variants of maximally parallel programs are constructed in the second step. Figures 2; references: 6.

UDC 681.3.06:51

PROGRAMMING ON THE SYNCHRONOUS MULTIPROCESSOR M-10 COMPUTER (SETTING UP A SYSTEM FOR MODELING PLASMA KINETICS

[Abstract of articles by Berezovskiy, M.A., Ivanov, M.F., Petrov, I.V. and Shvets, V.F.]

[Text] The article is devoted to questions of the design and realization of a deparalleled system for modeling multidimenstional physical processes using the synchronous multiprocessor M-10 computer. A well known computer model for plasma kinetics is analyzed, which is based on the macroparticles technique. Methods of deparalleling are described which were developed for the modeling stages and for input/output, which is matched to the speed of the modeling calculations. References: 10.

UDC 681.3.06:51

THE STRUCTURAL PLANNING OF SOFTWARE SYSTEMS FOR MINI AND MICRO-COMPUTERS

[Abstract of article by Yushchenko, Ye.L., Tseytlin, G.E. and Muchnik, M.M.]

[Text] Questions of the structural planning of the components of mini and micro-computer (MEVM) software are treated in the article. An approach is proposed which is based on the application of the tools of algorithmic algebra systems as the means of formalizing structured programs. The structural configurations of a typical assembler and macrogenerator are given. References: 10.

UDC 681.3.06

THE COMMON ALGOL-GDR MEMORY

[Abstract of article by Rvachev, V.L. and Matsevityy, A.M.]

[Text] The application of additional memory types in ALGOL-GDR is treated, where these simplify programming in this language. Figures 1; references: 3.

UDC 681.3.06

A MULTILEVEL MODEL OF THE ARCHITECTURE OF DATA BANKS AND INFORMATION RETRIEVAL SYSTEMS

[Abstract of article by Ilyushin, A.I. and Filippov, V.I.]

[Text] A model of data bank and information retrieval system architecture is described which is constructed in the form of a combination of levels of two hierarchies: "targeted", which reflects the overall structure of any subject region, and the hierarchy of "representations" of objects in the computer. As a result, the programming software for data banks and information retrieval systems can be treated as an aggregate of subsystems, which are ordered in the form of a two-dimensional table. Figures 2; references: 6.

UDC 681.3.01:681.3.06

THE 'EL'BRUS' SYSTEM

[Abstract of article by Babayan, B.A. and Sakhin, Yu.Kh.]

[Abstract] The article is devoted to a description of the architecture and software for a new family of high performance multiprocessor computer complexes: the "El'brus-1" (E-1) MVK [multiprocessor computer complex] and the "El'brus-2" (E-2) MVK, which were developed in the Institute of Precision Mechanics and Computer Engineering. Figures 3; references: 6.

UDC 519.712

A SYSTEM OF BASIC PROCEDURES FOR PROCESSING HALFTONE IMAGES

[Abstract of article by Levina, G.A. and Rakov, S.A.]

[Text] A method is proposed for the description of half-tone image processing algorithms. The method is based on the representation of the screen display image in the form of a matrix, the elements of which correspond to points on the screen. This method has been used in the development of the basic programming software for research automation complexes based on the process control computer complex of the international system of small computers having a trunk structure. References: 6.

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CSO: 1863

ABSTRACTS FROM THE JOURNAL 'AUTOMETRY'

Novosibirsk AVTOMETRIYA in Russian No 4, Jul-Aug 80 pp 117-120

UDC 681.327.8

MODEM IN THE CAMAC STANDARD WITH DIGITAL METHOD OF SIGNAL FORMATION

[Abstract of article by Fesenko, B. V., and Chernavin, A. D.]

[Text] The article describes a digital CAMAC modem intended for data transmission over a channel of tonal frequency and the principles of digital formation of a modulated signal with an assigned frequency spectrum. A structural diagram of the modem transmitter is presented, as are the results of simulation.

UDC 681.3.06

INTERMEDIATE-LEVEL LANGUAGE FOR CONTROL OF A CAMAC MICROPROCESSOR SYSTEM

[Abstract of article by Vlakhova, K. P.]

[Text] The IML language is intended for work with CAMAC systems in real time. The semantics of the language is determined by the Committee for Standardization on Nuclear Electronics and the syntax is connected with specific realization. This paper describes the syntax of an intermediate-level language for control of CAMAC systems by means of a series 6800 microprocessor.

UDC 681.3

SYSTEM FOR MICROPROGRAMMING AND DEMUGGING OF SECTIONAL MICROPROCESSOR DEVICES

[Abstract of article by Kasperovich, A. N., Mantush, T. N., Prokopenko, V. I., Sluyev, V. A., and Solonenko]

[Text] The article examines a system with a mini-computer (of class PDP-11) with general software and CAMAC hardware, used in the creation of sectional microprocessor devices. The system permits the debugging of microprograms and their recording in a PROM. The article describes the functioning of the system, the composition structure of its software, and presents functional diagrams of the principal modules

--the module for communication with the device being planned and the module for recording information in the PROM. The system programs are written in BASIC and Assembler.

UDC 621.372.54:681.327.8

MICROPROCESSOR SYSTEM FOR OPERATIVE GEOPHYSICAL EXPERIMENTAL DATA PROCESSING

[Abstract of article by Beresnev, V. K., Katruk, Yu. M., Rotachevskiy, B. M., Shchetinin, Yu. I., and Yunoshev, S. P.]

[Text] The article describes an operative geophysical information system constructed on a K584IK1 microprocessor. Calculations are made in real time of current estimates of the mathematical expectation and the mean-square error according to recursive algorithms, the use of which, besides reducing expenditures on equipment, provides the possibility of tracing error in measurements.

UDC 681.325.65

INTERACTIVE GRAPHIC COLOR CRT SYSTEM BASED ON A MINI-COMPUTER

[Abstract of article by Vasilevskiy, A. V., Gorobchenko, A. A., Zlotnik, Ye. M., Nagibina, O. F., Semenkov, O. I., and Shirokova, N. Ye.]

[Text] The question of constructing an interactive graphic system based on a mini-computer is examined. The structure and functional interaction of the main hardware of the system are presented. The system of display processor instructions is describe and its main characteristics are pointed out.

UDC 621.391.172:621.397.681.518.2

PATTERN PREPARATION IN AN INTERACTIVE MODE IN TASKS OF MEDICAL DIAGNOSIS AND INVESTIGATIONS OF NATURAL RESOURCES

[Abstract of article by Belikova, T. P., and Yaroslavskiy, L. P.]

[Text] Algorithms for the following methods of digital preparation of patterns are described: adaptive amplitude conversions, preparation with use of optimum linear filtration and location of objects on a pattern. An interactive operating mode is described and the results of using named algorithms to process mammograms and aerial photographic surveys of the earth's surface are presented.

UDC 681.3

CAMAC MODULE FOR CONNECTION WITH M-400 COMPUTER IN DIRECT MEMORY ACCESS MODE

[Abastract of article by Lebedev, N. S., and Mantush, T. N.]

[Text] A module of direct access to the M-400 memory is described, one which accomplishes a monopolar mode of data unit exchange through a CAMAC main-line crate.

The module functions jointly with the program exchange crate-controller, assuring an exchange rate of up to 400 K words/s. The structure of the direct memory access module and its interaction with the crate-controller and the main line COMMON BUS are shown.

[71A-2174]

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CSO: 1863

UDC 007.52

VISUAL INFORMATION PROCESSING IN ROBOTS

Moscow VIZUAL'NAYA INFORMATSIYA I ZRENIYE ROBOTOV in Russian 1979 (signed to press 29 May 79) pp 1-6

[Annotation, table of contents and foreword from book "Visual Information and Vision of Robots", by Georgiy Petrovich Katys, Izdatel'stvo "Energiya", 5,500 copies, 176 pages]

/Text/ The book examines the principles of construction of visual information processing systems, compares them, presents their basic characteristics and indicates their fields of application. It demonstrates the potentialities of visual information processing systems in enhancing the independence of robots and extending their capabilities and sphere of application.

The book is intended for engineering and technical personnel specializing in the field of automation, cybernetics and information processing problems.

Contents

Foreword

Extending the capabilities and sphere of application of robots at the present stage in the development of robot engineering is connected with the need for an intensive development of facilities for the perception and processing of diverse information on the environment and with providing robots with greater independence. It should be noted that the problem of information support for robots is of great importance in the general set of problems arising during the formation of the block diagram and general appearance of robots. At the same time, the attainable level of independence of robots largely depends on the depth of study of this problem. As is well known, in order to function normally in an unstable environment, an independent robot should perceive and process vast flows of visual, tactile, acoustic and other information. Visual information is of fundamental importance among this complex of information flows. The importance of visual information in the control of an independent system is confirmed by the fact that man receives about 85 percent of the information he needs through the visual channel.

It can be stated that visual analyzers are the main communication channels of robots with the external world through which the basic flow of information needed for their control is received. Therefore, the selection of rational principles of construction and optimization of the block diagrams and parameters of such devices, as well as the development of self-adjusting visual systems possessing properties of adaptation for the changing characteristics of the environment, are important tasks.

The book offered examines the set of problems and questions connected with different aspects of perception, processing and utilization of visual information for robot control. It considers the ways of selecting rational principles of construction of visual systems and methods of determining the parameters of the block diagrams of such systems. It analyzes various aspects of the perception and processing of visual information at different hierarchic levels of the visual analyzers of robots. In connection with the development of second- and third-generation robots intensive work on the production of visual systems capable of performing quite complex operations in the recognition of external objects and orientation among them has been carried out recently.

Various methods of information processing, including methods of monocular image processing and recognition, methods of stereogram processing, methods of dissection by a light lattice and others are used in the development of visual organs. The enumerated methods of analysis of visual information are examined in various chapters of the book.

Significant advances in the field of bionic investigations of the visual organs of animals have been made recently. At the same time, judging from literature and patent publications, the results of investigations make it possible to approach the development of technical devices modeling some functions of visual organs. The indicated facts prompted the author to examine this set of problems.

The book examines the results of bionic investigations of functionally original visual organs of some animals. Various aspects of perception and processing of visual information in the visual organs of living organisms, as well as the possibilities and ways of modeling certain functions of visual analyzers in engineering systems, are analyzed.

As is well known, a sequential selection, filtration and coding of visual information of value for an animal are carried out in the visual analyzer at its different levels. Such filters single out on images contours, straight lines and boundaries of a certain orientation, moving objects and so forth. Engineering models realizing some of the enumerated functions have been developed during the recent period. The book examines the functional and block diagrams of various attribute detectors (detectors of moving objects, contours, lines and so forth) and presents their parameters and characteristics.

Semiconductor, matrix and television technology combined with fiber and integrated optics is the technical basis for the realization of bionic principles of analysis and transformation of visual information.

On the basis of an analysis of the published data the author attempted to give one of the possible extrapolations of the future state of some trends in the development of visual systems of robots. This attempt was made on the basis of an analysis of patents, certificates of invention and various publications containing information on the possible trends in future developments. It should be noted that after some time these data will be reflected in the technical realizations of the systems of the examined category.

Unfortunately, at present there is no book that would generalize and analyze all the data on this problem published in periodical and patent publications. The book offered to the reader is to make up for this deficiency.

The book aims at giving the reader a general idea of the ways of and prospects for the development of a category of highly informative visual analyzers of robots, as well as of the ways of development and interaction of the basic trends in coherent techniques, techniques of space and time filtration of images, bionic mechanisms of processing, methods of recognition and modern methods of photoelectric analysis of images. The book presents a classification of the visual analyzers of robots and examines the principles of their structure, block diagrams and information characteristics. It indicates the possible ways of utilizing bionic principles of processing of visual information in the development of block diagrams of the visual analyzers of robots.

The material presented gives the reader a good idea of the various principles of construction of the visual analyzers of robots, methods of selecting rational block diagrams and ways of determining the parameters of such systems.

Assuming that this book is not free of shortcomings, the author thanks the readers in advance for all their remarks, which he requests be sent to the following address: 113114, Moscow, M-114, Shlyuzovaya nab., 10, Izd-vo Energiya.

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CSO: 8144/0017

DIGITAL CONTROL SYSTEMS

Kiev KIBERNETIKA I VYCHISLITEL'NAYA TEKHNIKA: DISKRETNYYE SISTEMY UPRAVLENIYA in Russian No 49, 1980 (signed to press 5 Sep 80) p 97

[Table of contents from collection "Cybernetics and Computer Technology, No 49: Digital Control Systems", edited by Z. A. Maydan, Izdatel'stvo "Naukova dumka", 1,000 copies, 100 pages]

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CSO: 1863

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INFORMATION GATHERING AND TRANSMISSION

Kiev OTBOR I PEREDACHA INFORMATSII in Russian No 62, 1980 (signed to press 4 Dec 80) p 118

[Table of contents from collection "Information Gathering and Transmission", edited by Z.A. Maydan and N.M. Trush, Izdatel'stvo "Naukova dumka", 1000 copies, 124 pages]

[Text] Contents Page

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UDC 616.8-091.81(088.8)

PROBLEMS AND PROSPECTS OF DEVELOPING NEURON TECHNOLOGY

Kiev OTBOR I PEREDACHA INFORMATSII in Russian No 62, 1980 (signed to press 4 Dec 80) pp 49-55

[Article by V. L. Kuznetsova, V. L. Kuz'menko and I. M. Tsygel'nyy, L'vov, from collection "Information Gathering and Transmission", edited by Z.A. Maydan and N.M. Trush, Izdatel'stvo "Naukova dumka", 1000 copies, 124 pages]

[Text] The progress of modern computer technology is determined by a combination of two trends--improvement of the component base by using new advances of physics and technology and intensification of the search for new theoretical fundamentals of realization of computer devices to which multiple-digit [17] and neuronal [5] logic is related. The desire of investigators to combine the advantages of both trends led to intensive study of the principles of processing the information of the human nervous system and to attempts to utilize these principles to develop computer devices. One can assume that some computers will be constructed on principles of information processing and storage in the human brain on the basis of components which simulate the behavior of the nerve cells and of neuron networks of them. Modern computers are usually designed to solve formalized problems. An advantage of devices based on neuron networks is the possibility of solving unformalized problems related, for example, to pattern recognition or to control of complex behavior in a probabilistic-stochastically variable medium. The main distinguishing feature for these computers will be the capability of self-organization and self-programming and possibly the capability of alogical decision-making, i.e., making decisions in alternatives having equal probability. The experience of the evolution of biological structures can be used in constructing them. Of course, we are not talking about blind copying of the working principle of nervous system networks. On the contrary, the paths of evolution of colloidal systems are very limited and the problem is to proceed further than biological evolution, i.e., those types of neurons may appear in models of brain systems which do not occur in the natural analog (if these forms are required to develop more improved computer systems) or which have not yet been discovered.

A large number of neuron models have now been developed in the USSR and abroad, among which models of nerve networks used in computer technology, automatic control systems, information transmission and processing systems, pattern recognition systems and so on can be compiled. Since many of them are inadequately effective from the viewpoint of information processing in the neuron, the general criteria of the optimum construction of circuits of neuron-like components must be refined, which permits one to denote methods of neuron modelling occurring at present.

Construction of neuron-like components required that two problems be solved. The first is development of high-speed electronic models of the neuron system to study its behavior in those cases when the capabilities of ordinary methods of electrophysiology are limited (for example, in study of networks that process sensory information, in decoding the mechanisms of internal storage, in construction of models of the pathology of the nervous system for diagnosis and so on). Solution of these problems in itself justifies the expenditure of efforts to develop a wide range of neuron models but far from exhausts the capabilities of using them.

The second problem is to use neuron-like components and networks of them in technology.

According to the postulated problems, two approaches were noted in the principles of constructing neuron-like components and networks. The first, historically earlier approach is determined by the desire to copy maximum analogs as closely as possible [2, 20, 24] with reproduction of the physiological properties of the neuron as well as the information properties. The second approach includes modelling of the components of the nerve network as information processing systems [12, 15]. One is justified in talking about neuron technology in this case.

The term "neuron technology" means the use of the principles of information processing in the neurons and neuron networks to develop electronic devices. Unlike neurocybernetics, a primarily theoretical science, neuron technology is concerned with problems of a practical nature and without linking itself by direct imitation to the biological analog, it attempts to solve problems of using this analog for purely technical purposes.

The need to separate the approaches--"neuron modelling" and "neuron technology"--is determined by the fact that they belong to different branches of science: the first belongs to biology and physiology while the second belongs to bionics, i.e., neuron technology is a branch of bionics which utilizes the principle of information processing in the neurons for development of hardware.

Several trends in the development of neuron technology have now been noted. One of them assumes the development of universal neuron-like components which would provide for construction of networks of any degree of complexity, being limited only by similar models [12, 15]. This trend is apparently more promising since it is the most technologically effective and leads to universality of components and units of neuron technology.

Another trend provides for introduction of components into the structure of neuron networks that are different from the basic structural unit--the neuron-like component. Thus, a model of a neuron network containing and additional random number generator, control block, flip-flop block and timing pulse generator is presented in [12]. It should be noted here that the homogeneity and regularity of the structure are of important significance in realization of supercomplex neuron networks, as well as in realization of any complex measuring information systems. These requirements acquire special significance when converted to microelectronic technology. Realization of the necessary functions of these blocks by a set of neurons rather than introduction of additional blocks into the network is effective in this regard.

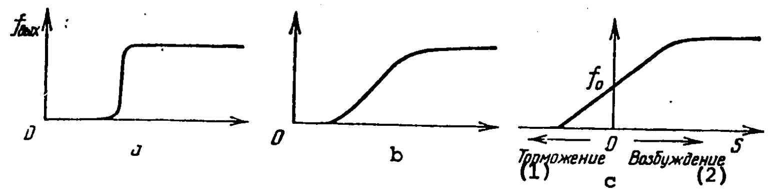
Neuron models are developed rather frequently in which the authors attempt to reproduce in a single model the maximum properies inherent to the neuron. The model frequently contains components which determine the execution of functions that are unnecessary at first glance (for example, the effects of nonlinear increase of the frequency of the converted signal which provides sharper response to variation of input signals [12], damping of input signals and so on) and that significantly complicate both the model and the nature of the information transformations. However, the given circuit solutions can significantly increase the operating efficiency of the neuron network in solution of unformalized problems.

The trend related to development of neuron-like components based on a minimum number of components also merits attention. These may include neuron-like components [4, 25]. The history of development of this trend illustrates the helical development of neuron technology. The first neuron-like components [19,22] were developed in simplified form by weak development of the technology and electronics in a given historial time segment. Ever more complex and cumbersome models were subsequently developed for more accurate reproduction of the information properties of neurons [20]. They could not be used in construction of complex networks. The number of components required to develop a neuron-like component is reduced in the next step of development of neuron technology. In this case, "shortening" it was determined by the use of components which carry more information properties and the effectiveness of these components is manifested by internal physical processes (avalanche transistor, thyristor [4], tunnel diode [25], multigate transistor, liquid crystal) and so on, rather than due to circuit solution. Modern integrated circuit technology can be used to develop these neuron-like components. "Simplification" of neuron-like components may be of special significance, we feel, upon transition to the use of these components as a component base for molecular and supramolecular cybernetics. In this case the joint use of modern developments of the physics of supramolecular structures and neuron technology may determine the development of self-developed dynamic cybernetic systems.

Development of integrated circuits of neuron-like components based on an optimum set of circuit components is also timely.

However, the purpose of developing neuron technology is to develop hardware which may find application in the national economy rather than in construction of neuron-like components. It is natural and feasible to use models of neuron networks constructed from neurons rather than a neuron model to develop these devices. One should take into account when constructing models of neuron networks that the formation of existing neuron networks is stochastic [7, 16] along with the rigid three-dimensional structure of neuron-neuron links [16] caused by morphogenesis, while spherical networks are formed for solution of specific problems. In this case each neuron may function at different times in several networks. It follows from this that qualitatively new components or modifications of existing neuron models are required to develop a dynamic structure of neuron networks. One of the papers in the given direction is the network model suggested by Pak [12], which consists of neuron-like components having inputs capable of changing their function and which permit one to achieve stochastic organization of the signal circuit in the network.

A sufficient number of types of neuron-like components with qualitative specialization to perform complex functions has not yet been developed for construction of



Key:
1. Inhibition
2. Excitation

complex neuron networks. It is known that the nervous system contains more than 1,000 different types of neurons [13] with presently determined morphological differences, which does not exclude functional differences. There is a need in this regard to find new functional solutions of neuron-like components. Neuron models which provide the required diversity may include models of identification neurons, distributing neurons, innovation neurons, comparison neurons and other special neurons, the appearance of which should facilitate the problem of constructing complex networks.

We feel that the use of the principles of organizing multi-digit components and structures is promising in the given direction for development of neuron-like components and networks [9, 17]. It is shown in [6, 10, 23] that a neuron is described not only as an analog but also as a threshold digital component. Based on our investigations, one should note that the processes of information conversion in existing neuron-like components can be described by one of three principles f(S) shown in the figure, a, b and c, where $S=\sum_{i=1}^{n} a_i f_{\text{возб}} - \sum_{j=1}^{m} b_j f_{\text{торм}}$, f_{vykh} is the frequency of the pulse sequence at the output of the neuron-like component, f_{vozb} and f_{torm} are the frequencies of the pulse sequences at the exciting and inhibiting inputs, respectively, f_0 is the frequency of spontaneous activity, a_i is the weight of the exciting inputs and b_j is the weight of the inhibiting inputs. The characteristics shown in the figure, a, describe a threshold logic component operating on the principle of "all or nothing." The characteristic of a component of infinite-digit logic with lower and upper thresholds is shown in the figure, b. The figure, c, is the characteristic of a similar component, but one having spontaneous activity, which increases the sensitivity of the component and expands its capabilities.

It becomes possible to construct neuron networks with rearranged information structure, operation of which can be described by using multi-digit logic, upon introduction of some additions to the circuit of a neuron-like component, which may include, for example, quantification of the working frequency range. The neuron has a set of exciting and inhibiting inputs with weight coefficients ω_i and a single output. The input x and output y values vary upon corresponding normalization in the following range: $0 \leq x \leq 1$ and $0 \leq y \leq 1$. These values simulate the neuron signals--the pulse recurrence frequency--and do not change the sign. Moreover, the neuron has a lower and upper excitation threshold. Consequently, this operation can be described by the expression [5]:

$$y = \sum_{i=1}^{n} \omega_i x_i - \theta,$$

where θ is the threshold that, upon conversion to the arithmetic form of representation [18], yields

$$y(x_1, x_2, \ldots, x_n) = (\theta + 1) \& \sum_{i=1}^{n} \omega_i x_i - \theta \& \sum_{i=1}^{n} \omega_i x_i$$

and is similar to the arithmetic form of representation of a multi-digit logic function [18]. There were attempts to realize these models in [9, 21].

The logic of developing modern electronics also dictates the development of neuron-like components on the basis of digital technology, which specifically provides a significant increase in the accuracy of the information transformations in them and an increase of speed. Attempts to move in the given direction were undertaken [3, 14], but more intensive developments are required to achieve significant results which permit solution of the problem of constructing complex neuron networks that emerge as self-organizing systems capable of making independent decisions even under conditions of a scarcity of information, i.e., under conditions of rather high uncertainty,rather than as intermediate steps of information processing of the perceptron type [11].

The main principles of design organization and self-organization of these networks are required here.

The first principle is a sufficiently large set of components contained in the network. A set is required to provide the possibility of signal fluctuations. If fluctuations are undesirable in a system operating by a rigid program, they are required in a supercomplex system capable of unforeseen actions. This is determined by known information principles [1].

The second principle is the capability of the network for self-formation of feedback cycles. It must be noted that two neuron feedback cycles are distinguished: homeo- and heterostatic, which can apparently be mutually transformed. The designation of homeostatic cycles (neuron networks joined by negative feedback) is to maintain equilibrium within a given program. Heterostatic cycles (neuron networks with negative and positive feedback having aperiodic fluctuating activity) probably play a significant role. The operating rhythm of neurons of a heterostatic cycle depends on a large number of factors. Fluctuation of the rhythms of the system may acquire an exceptionally individual character as a function of the joining of primary (homeo- and heterostatic) cycles to second- and third-order cycles. The external effect achieved from receptor models may have an organizing effect on the rhythm of a supercomplex network in this case.

Assigning an input program to the system is also important. The presence of an input program is determined by the need to compare newly incoming information to it. The input program should obviously be similar to the genetic program or to the instinct in a biological system and should be determined by the properties of the system, but it may also be controlled externally.

Modelling of the system's own needs and its "attitude" to external effects are also required for development of self-organization conditions since a system devoid of these properties cannot be developed. For example, the system may be given the need to balance homeostasis under saturation conditions.

Thus, problems of neuron technology, as a field of bionics, are extremely interesting and vast. This is first development of a wide variety of input components (neurons and universal network cells) and second it is development of cyclic blocks of increasing complexity and hierarchical systems.

Solution of these initial problems of neuron technology will be possible during the next few years. With regard to subsequent development of organization of complex and supercomplex networks, it will obviously occur after a basis has been developed for integrated technology of the components of neuron networks which include a large number of neuron-like components joined into cyclic blocks. Considerably more promising is the use of the internal information properties of materials in those cases when the latter coincide to a specific degree with the properties of neuron structures. For example, these properties have a hierarchical system of supramolecular connections in polymers.

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HIGH-SPEED MEASURING SUBSYSTEMS

Riga SKOROSTNYYE IZMERITEL'NYYE SUBSISTEMY in Russian (signed to press 24 Jul 80) pp 4, 183-184

[Annotation and table of contents from book "High-Speed Measuring Subsystems", by Yuriy Nikolayevich Artyukh, Vladimir Alekseyevich Bespal'ko, Valeriy Yakovlevich Zagurskiy and Eduard Aleksandrovich Yakubaytis, Institute of Electronics and Computer Technology, Latvian SSR Academy of Sciences, Izdatel'stvo "Zinatne", 1,000 copies, 184 pages]

[Text] Measuring subsystems represent one of the varieties of user machines in the configuration of the computer network, oriented toward direct contact with the object of measurement, checking and control. A combination of stage and main principles of interaction of components is used in the considered version of the subsystem interface which permits realization of the function of the user machine by the subsystem while preserving the flexibility of its structure.

The main problem in design of the subsystem components is analog-digital conversion. The principles of optimizing the structures of different types of high-speed converters (tens of megabytes per second) are determined on the basis of its thesaurus. Phase representation of the signal is considered as the primary representation for frequency-time parameters, which permits one to select readout from time scales as the common method of converting them. The method permits one to achieve subnanosecond resolution while retaining high relative accuracy. Examples of the typical subsystem oriented toward analysis of a broad class of single signals and of a specialized subsystem of a laser flow velocity doppler meter are presented. The systems permit complete automation of scientific and industrial experiments.

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